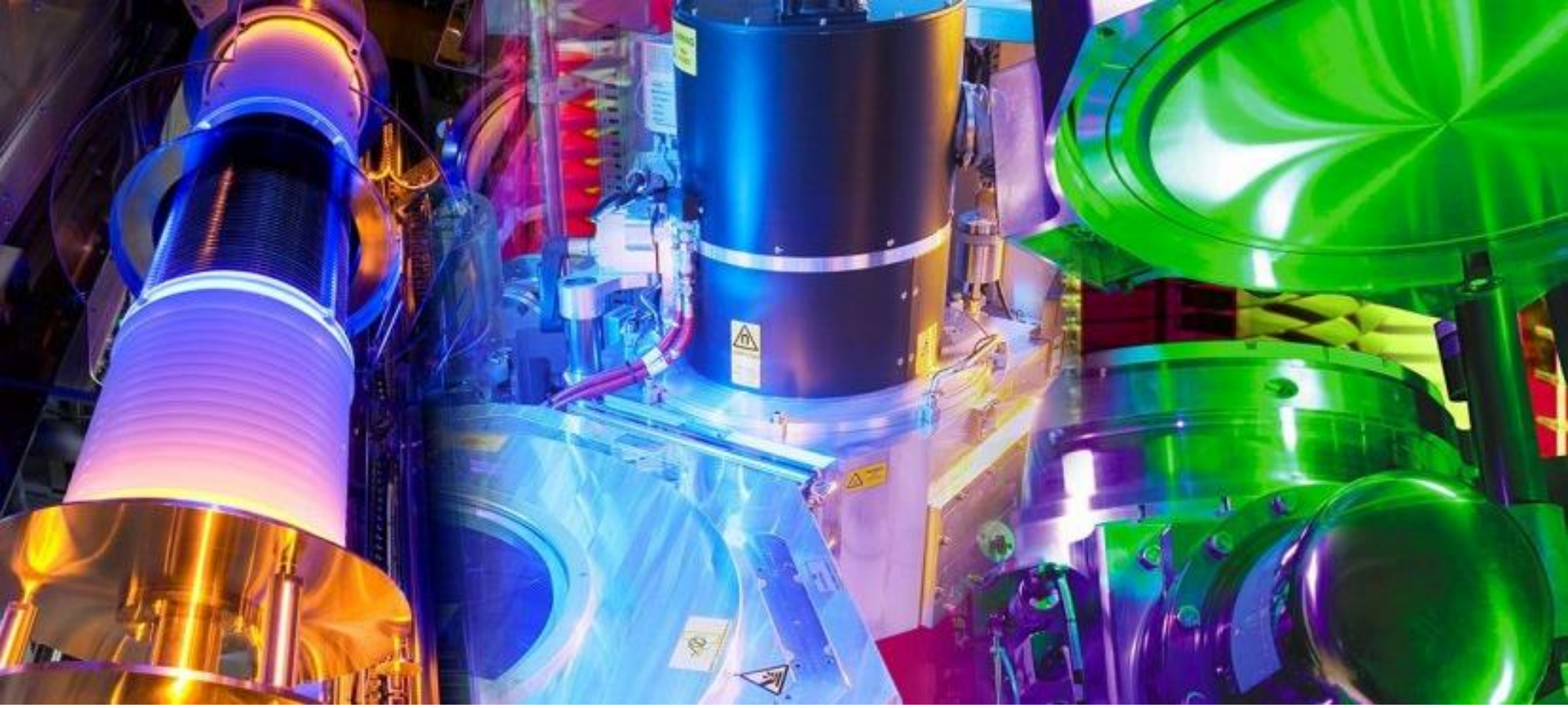

High Productivity UBM/RDL Deposition By PVD For FOWLP Applications

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October 19, 2016

2016 IWLPC 13th International Wafer-Level Packaging Conference

SPTS An orbotech. Company

Contents

- The rise of FOWLP
  - Why it's needed
  - Examples
  - Market growth
- PVD processing of FOWLP
- Challenges
  - Contamination
  - Particles
  - Cu exposed area
- Solutions

The Interposer Gap: Line & Space

High Cost

PCB Substrate Manufacturers

OSAT / Wafer foundries

Silicon

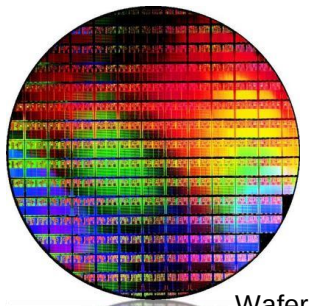
Glass
Who manuf interposers?
Ground rules ?

Opportunity

eWLB: <10um L/S
TSMC InFO: <5um L/S
RDL first FO: <2um L/S

FanOut

GAP!



Wafer Design Rule

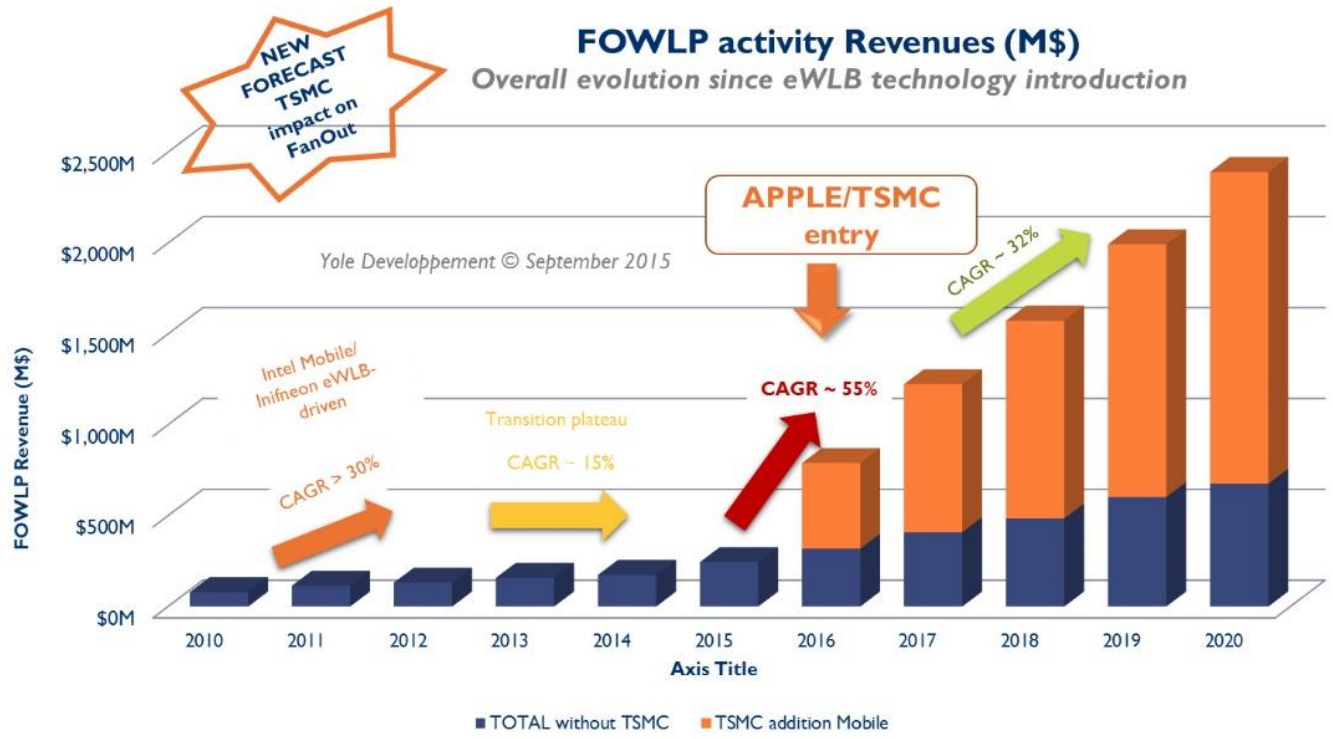
Organic Substrate

Lower cost than Si/Glass Interposer ?

100µm 25µm 10µm ~8-> 5µm 1µm 100nm 10nm

Courtesy Phil Garrou, Yole

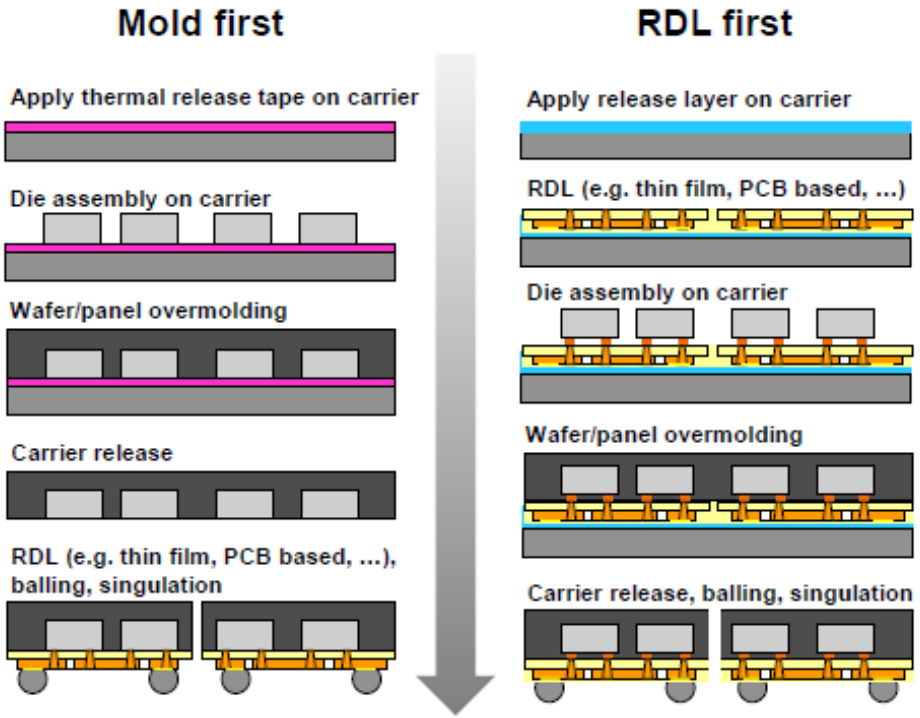
Fastest Growing Packaging Scheme



- Mobile is the main driver
  - Automotive, medical, industrial all active
- Massive influence from TSMC InFO
  - CAGR 32% through 2020, was 15%
  - WLP ~ 10%, FC ~15%

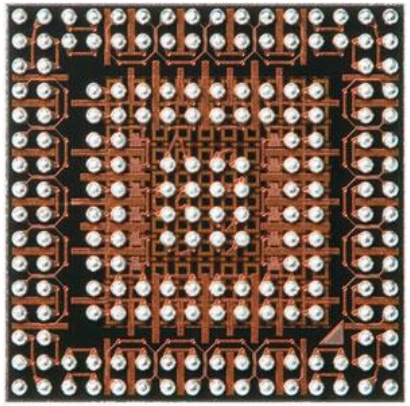
FOWLP Basics

- Enables WLP where BGA requirements exceed available footprint
  - Remove BGA laminate interposer substrate from the package
  - Reduce package height, reduce cost, improve performance
- Single and Multi-Chip Modules possible



FOWLP Examples In Production

- Original Infineon eWLB, Single Die
  - Wireless Baseband SoC (GPS, FM Radio, BT)

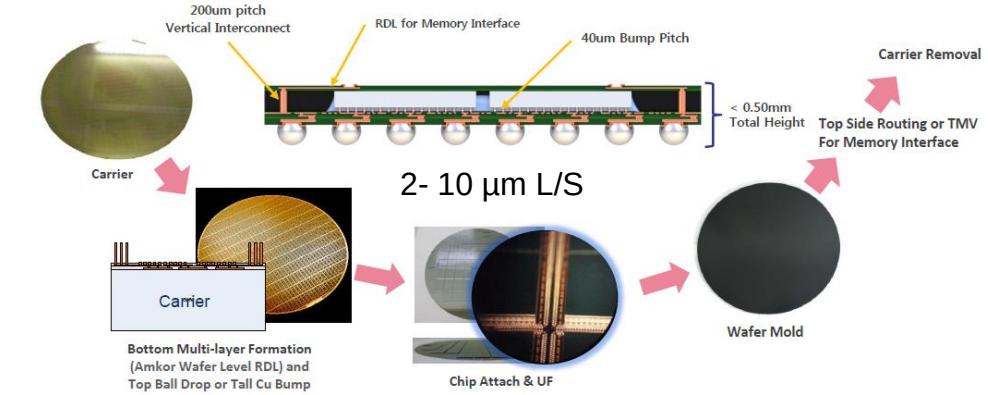


- Multi-Chip Modules, Integrated Passives

  - 10 µm L/S
  - Up to 3 Metal Levels (2 x RDL, 1 x UBM)

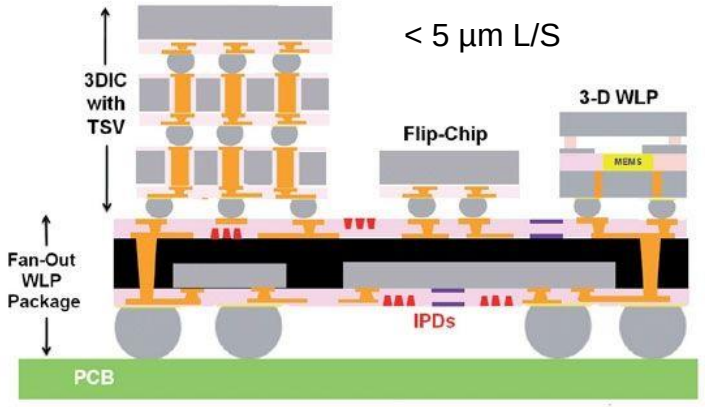
Increasing I/O Density

Amkor SWIFT [Silicon Wafer Integrated Fan-out Technology]

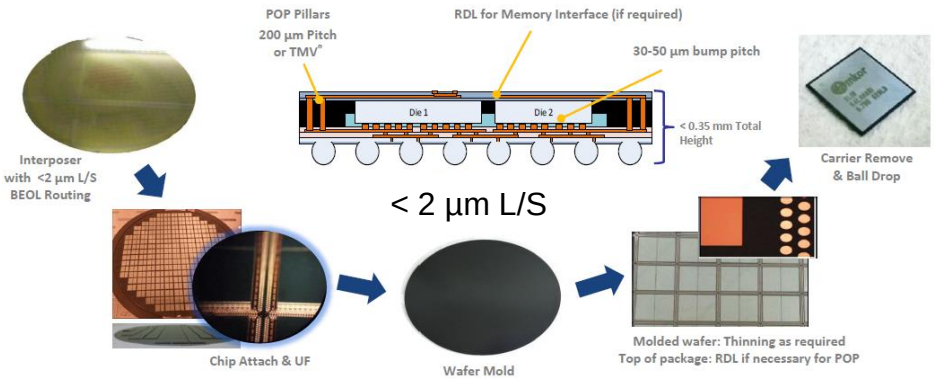


Courtesy of Amkor

TSMC InFO [Integrated Fan-Out]

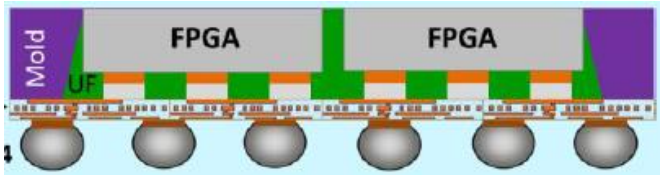


Amkor SLIM [Silicon-Less Integrated Module]



Courtesy of Amkor

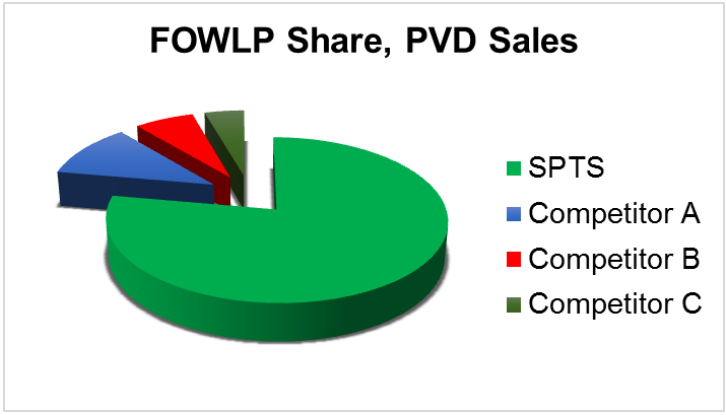
SPIL SLIT [Silicon-Less Interconnect Technology]

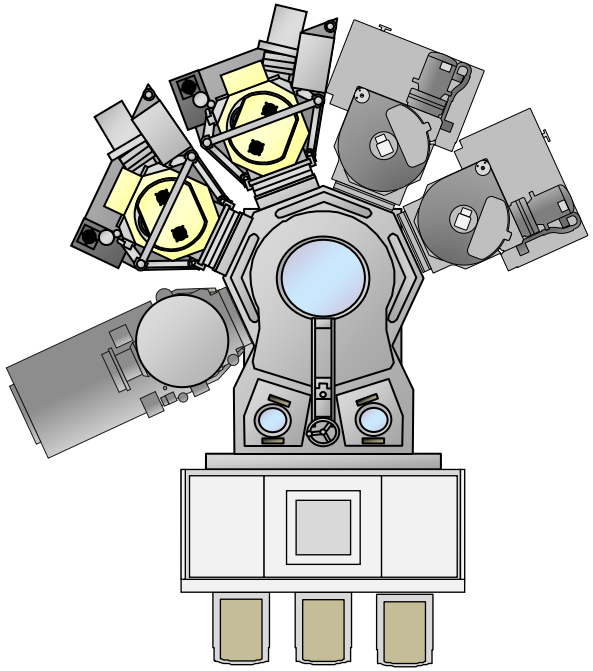


Fan-Out Programs in OSATs & Foundries Increasing

Sigma *fx*P FOWLP PVD System

- PTOR for original eWLB R&D
- HVM since 2009
  - >> 1M wafers processed
  - 200 mm, 300 mm & 330 mm
- Multiple customers:-
  - R&D, Production





FOWLP RDL Challenges for PVD

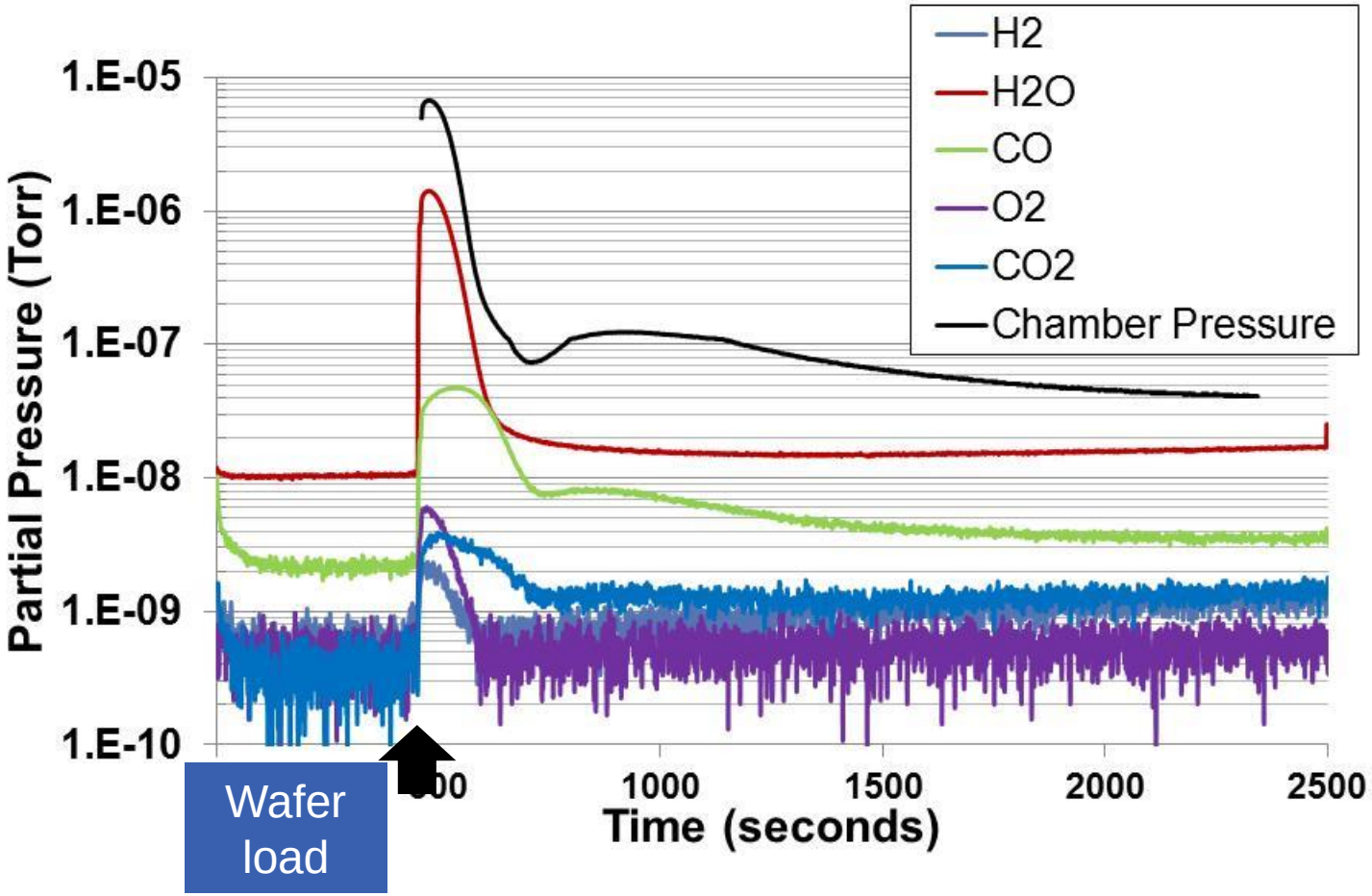
- FOWLP RDL Process Flow:-

Step	Detail	Comments
PVD	Degas – Etch – Ti or TiW – Cu Seed	T < 120C
ECD	Cu Electroplate	
Repeat for each UBM/RDL layer required (with dielectric deposition/patterning)		

Multiple challenges for PVD:

- Contamination: mold contains moisture, solvents
  - Must be removed before metal dep otherwise high Rc
  - Problem: mold wafer max temperature is low, <150°C
- Particles
  - Organic dielectrics commonly used in packaging; PBO, PI
  - Problem: C by-products can flake from chamber furniture after pre-clean
- Large Cu exposed area on top RDL
  - Problem: stops RF penetration in ICP etch chambers
- Mold wafer not flat, high value, 100% Known Good Die (KGD)
  - Wafers bow up to 7-8 mm in either direction, particularly MCM

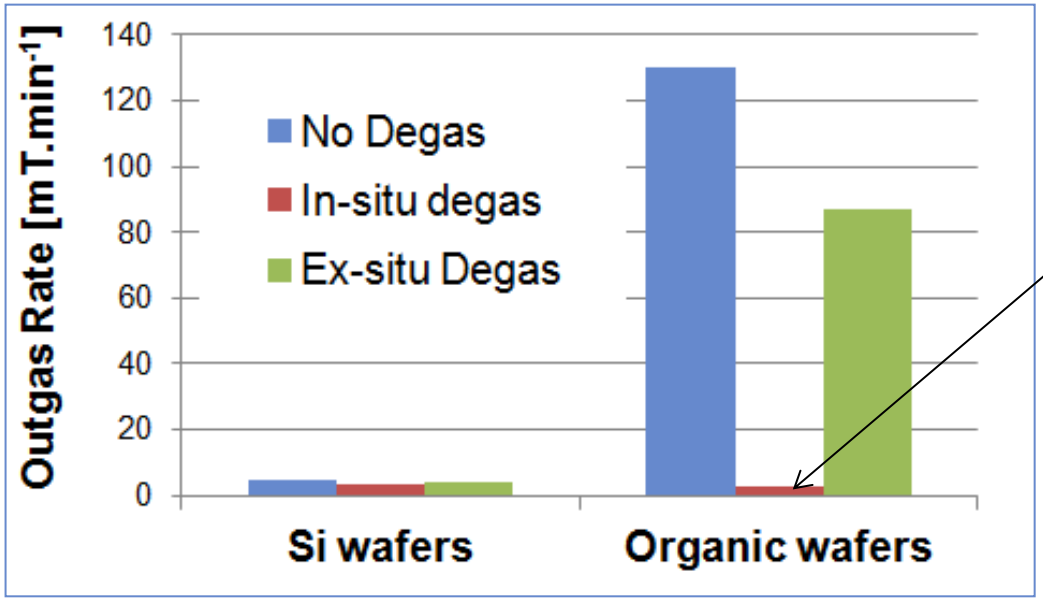
Mold Contains Contaminants



- Water and CO dominate
- At 120C, takes @30mins for gases to approach pre-load values
- How manage and still be productive?

Degas Under High Vacuum Is Key

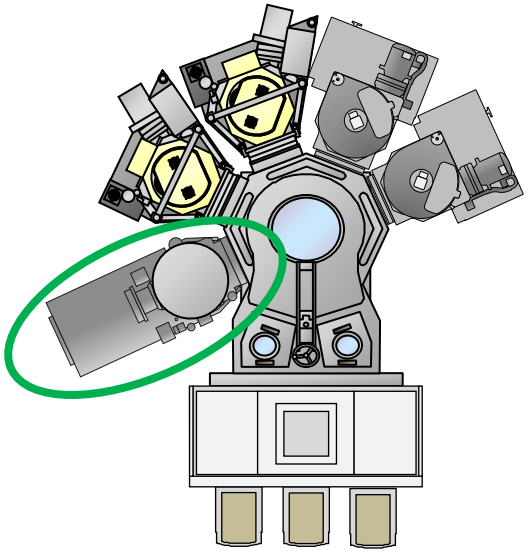
- To achieve lowest Rc, highest yield, degas under vacuum
- Degassing ex-situ and move to PVD system less effective
  - Mold quickly re-absorbs
  - Changes in transfer time will cause variable results

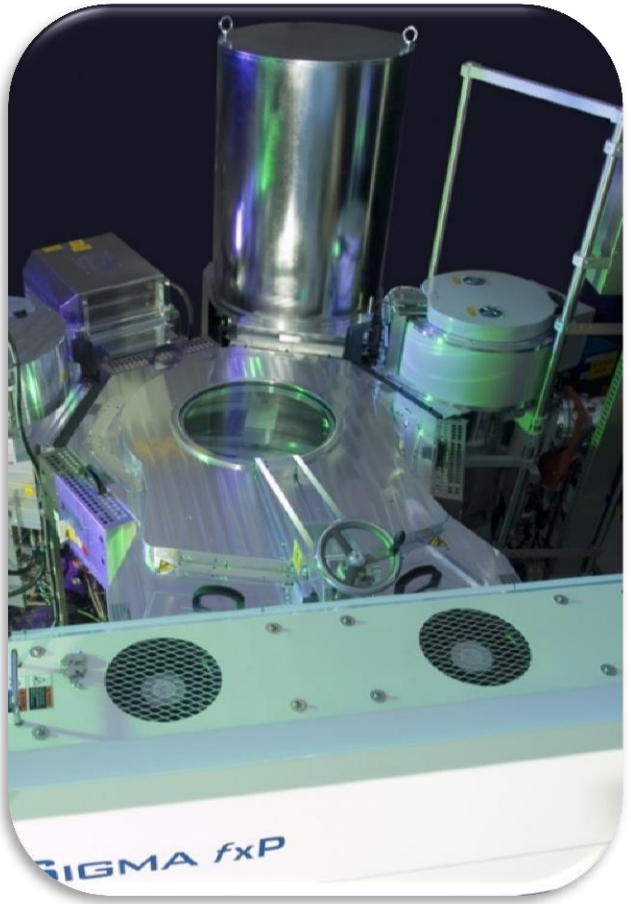


In-situ degas design ensures lowest outgas rates

T’put Advantage Using MWD

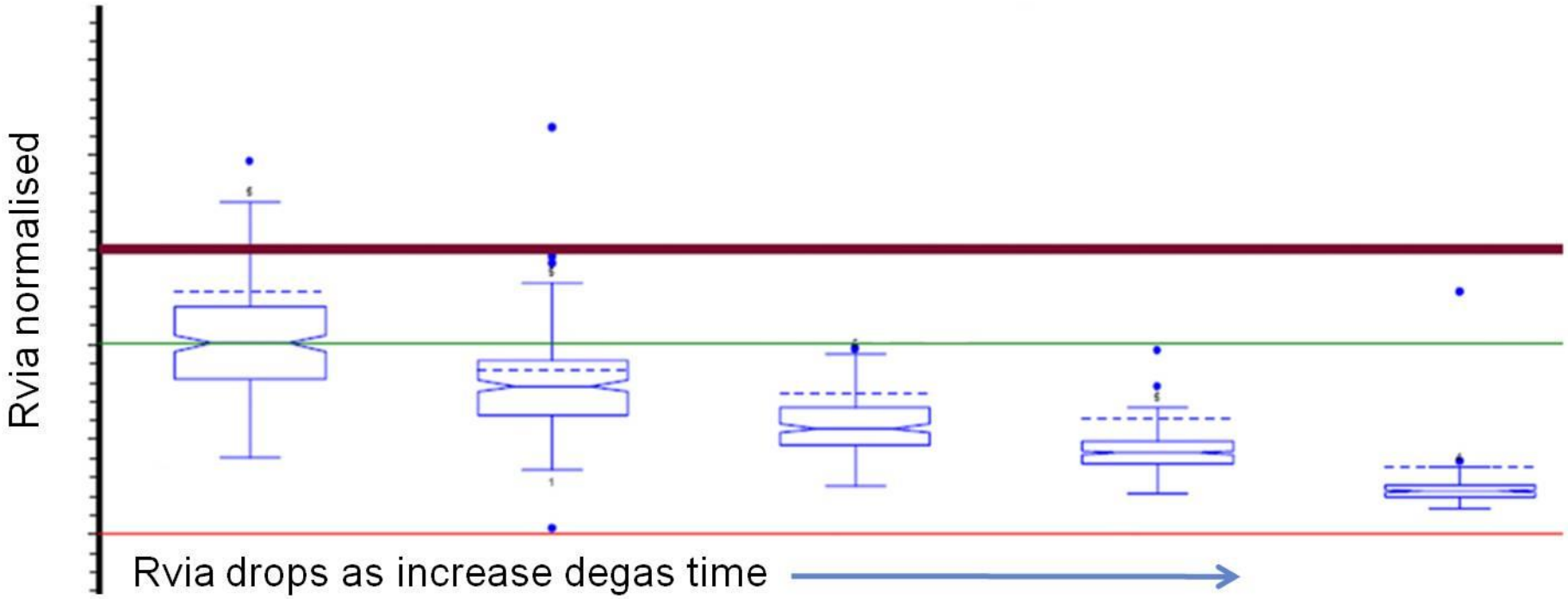
- Mold contains moisture, and has low temperature tolerance
  - Must degas for long time = throughput bottleneck
- Solution = Multi-Wafer Degas (MWD)
  - Batch concept, removes degas bottleneck
- Cryopumped for water efficiency
- Attached to the high vacuum side
- Complex scheduling software
  - Manages batch/single wafer interaction





High Throughput, Low Rc

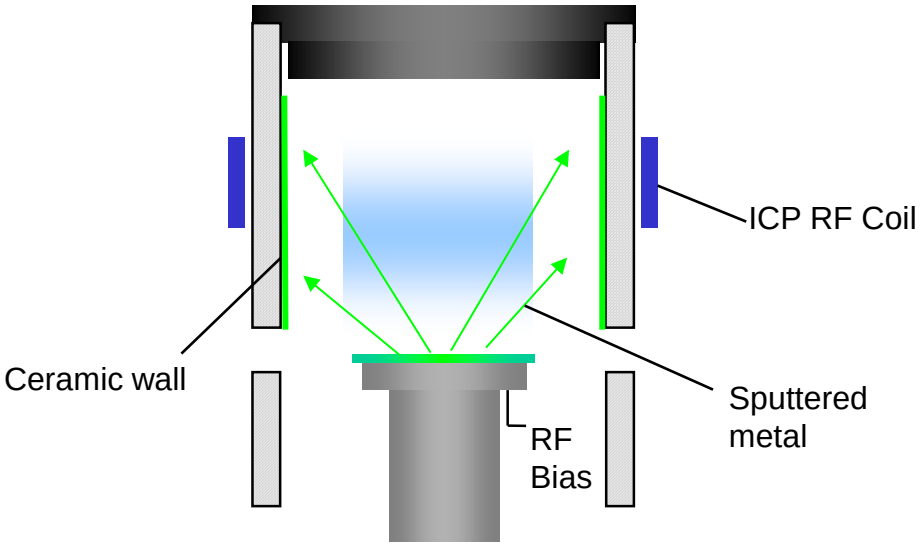
Tests performed on FO-WLP Test Vehicle
TMAX = 120C

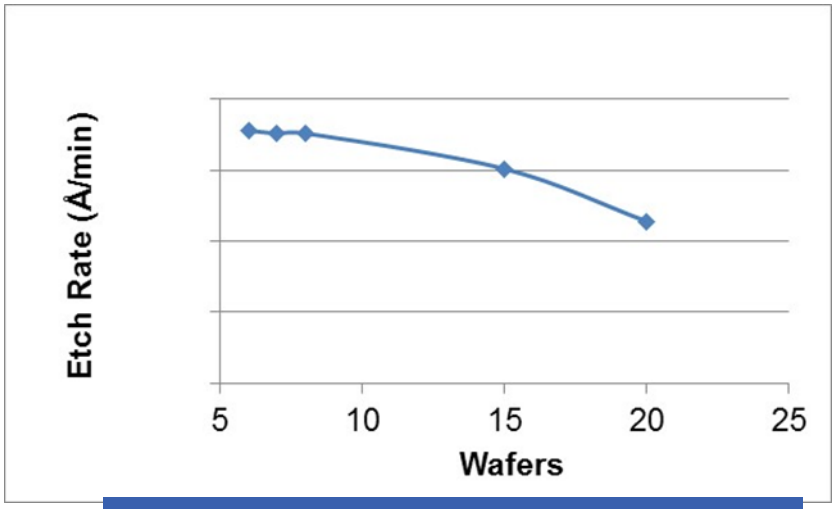


Individual wafers get long degas
Degas in parallel means t'put stays high

Dealing With I/O Density Increase

- FOWLP I/O density increasing, reduced L/S patterning
  - Increasing area of exposed metal
- In an ICP pre-clean, metal deposited onto the ceramic will block RF
  - Plasma eventually turns off



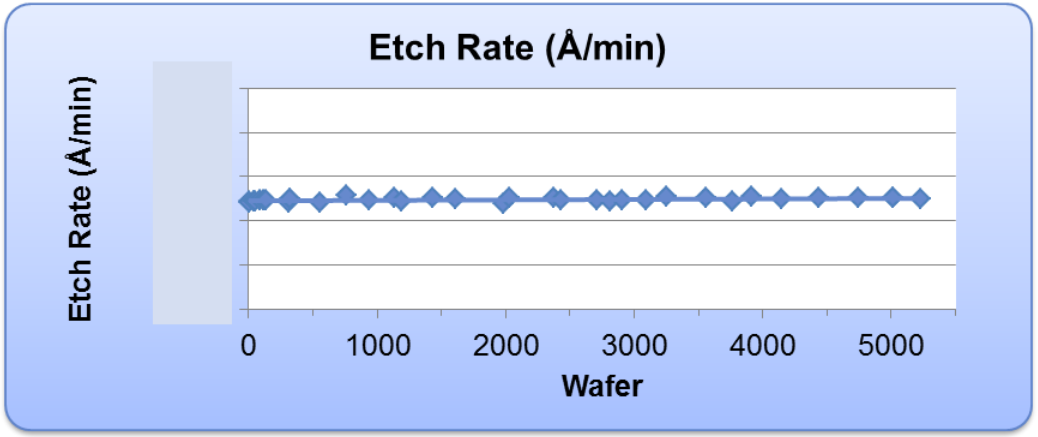


High exposed Cu on Standard ICP
Cu builds up on ceramic wall
Etch rate falls away

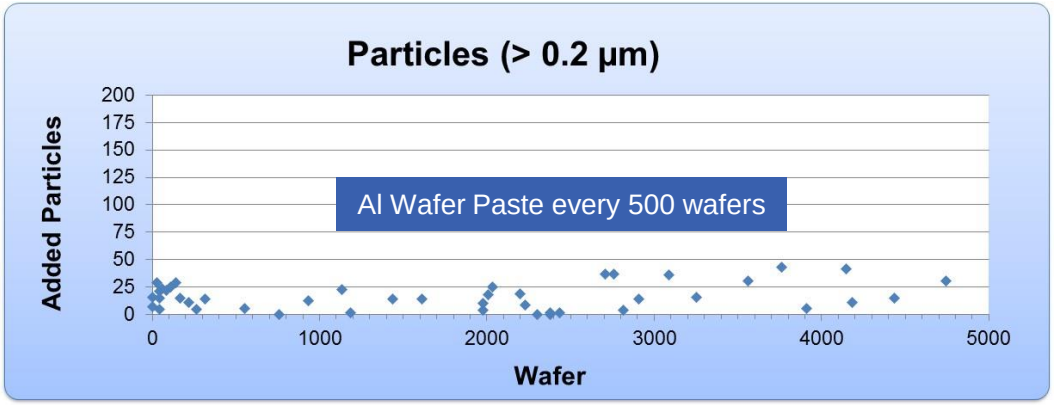
- How do you keep the lights on?

SE-LTX Solution

- Modified design prevents continuous band of metal forming on the wall
- Stability maintained over 5000 wafers

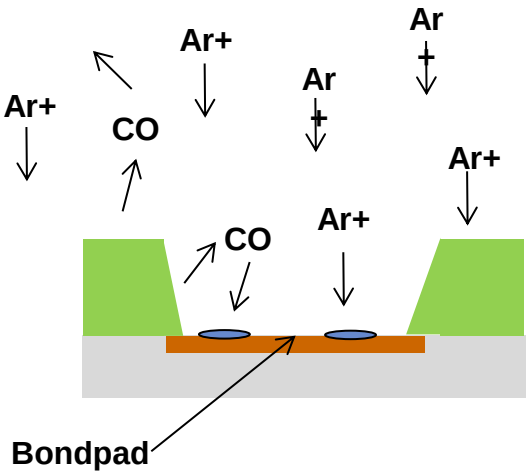


- PLUS allows metal pasting for PI/PBO particle control…



Keeping Rc Low

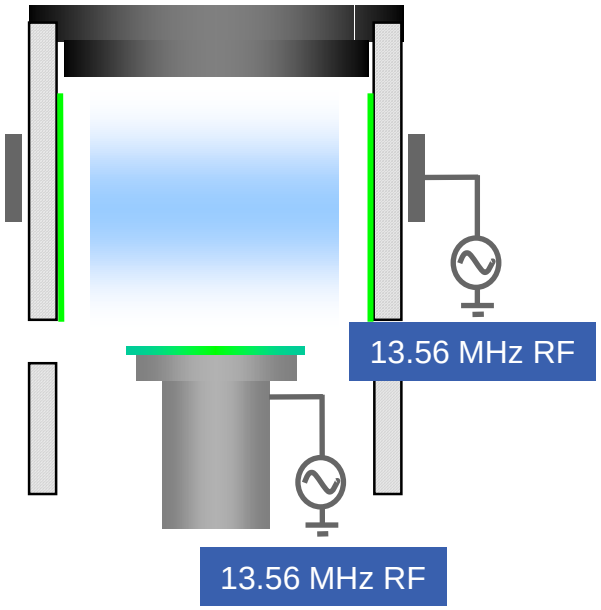
- Polymer dielectric passivation
  - PI, PBO, BCB, WPR
- Ion bombardment during pre-clean
  - Removes native oxide from bondpad
  - But also...breaks down polymer crust
  - C by-products and moisture released
  - Pad metal becomes contaminated
  - Rc increases



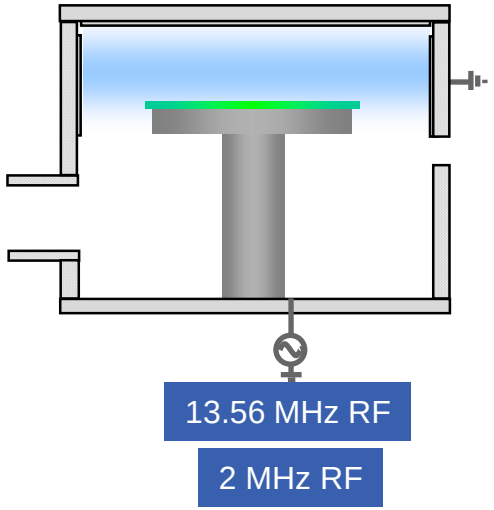
- Shrinking CDs increase the challenge

Why ‘Soft’ ICP Etch Is Best for Rc

ICP Etch

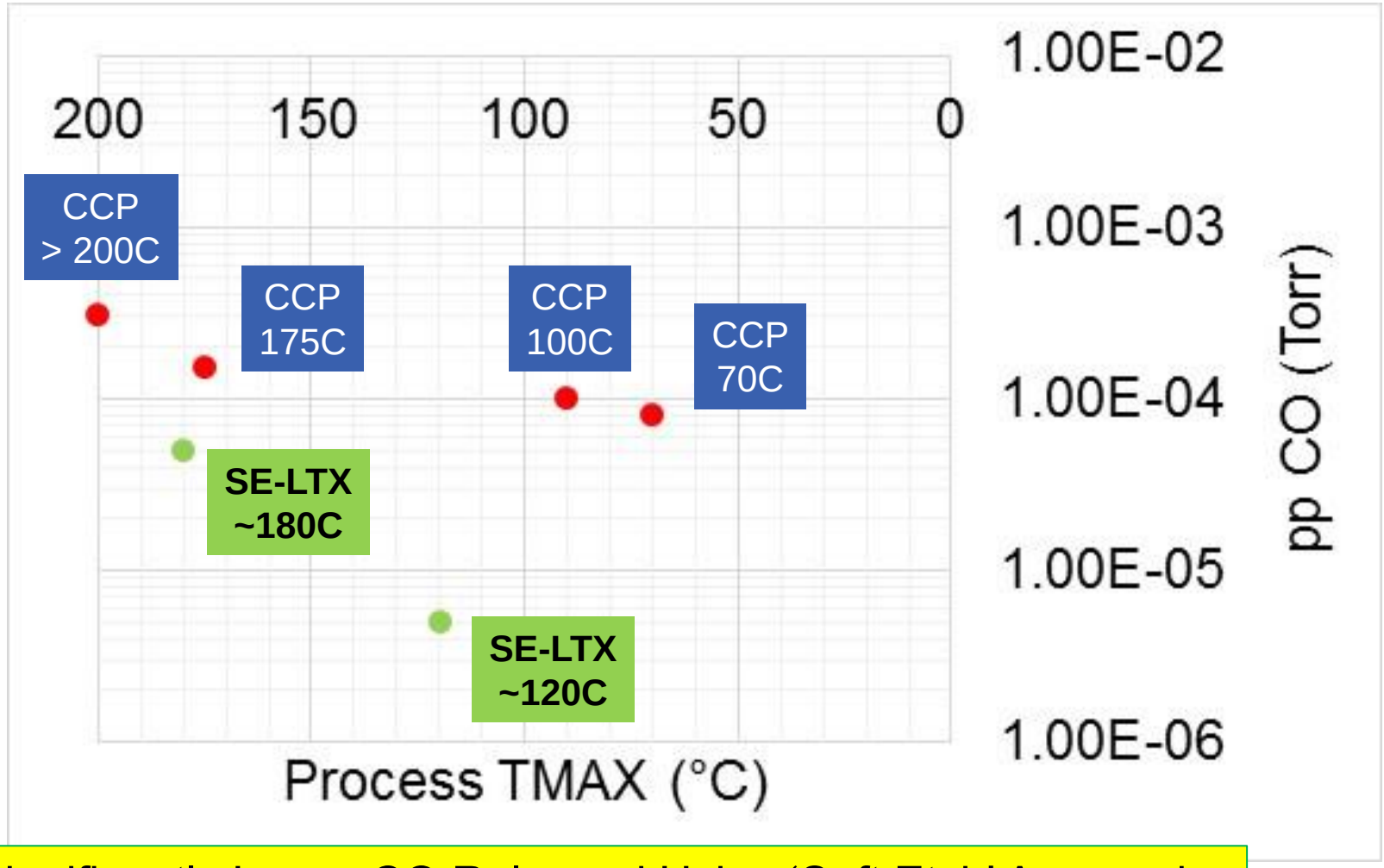


CCP (Diode) Etch



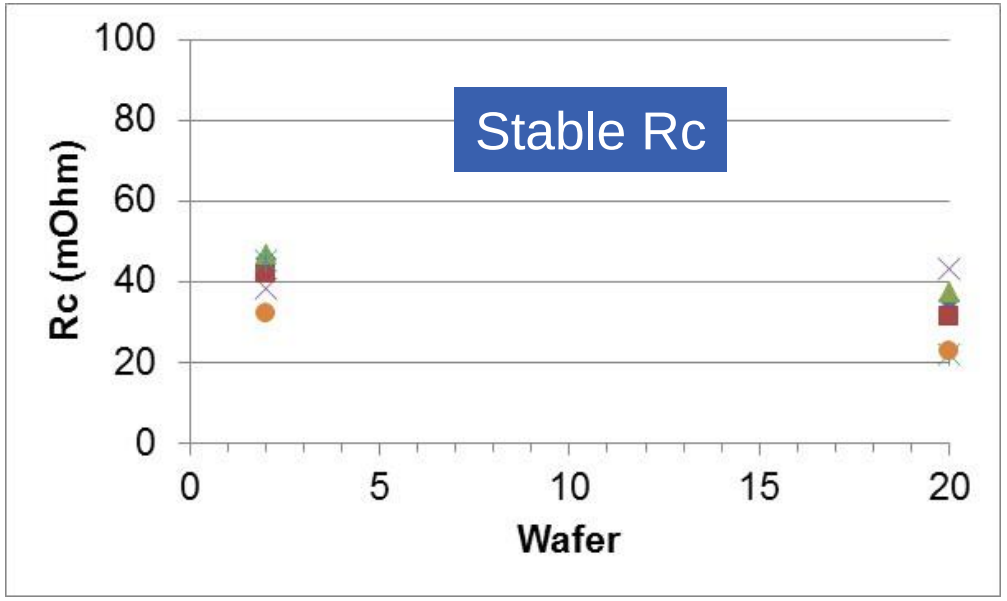
	ICP Soft Etch	CCP (Diode) Etch
DC Bias	- 400V	- 4000V
Ion Energy	Low	High
CO Release During Etch	Low [~E-05 Torr pCO]	High [~E-04 Torr pCO]

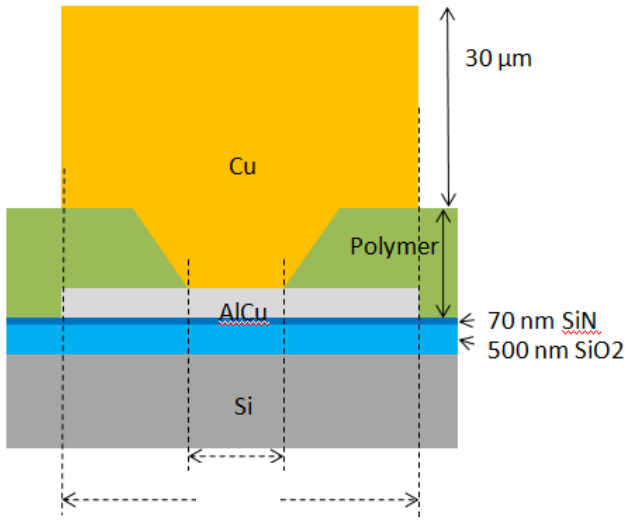
Soft Etch CO Peaks vs Diode Etch



Significantly Lower CO Released Using ‘Soft Etch’ Approach

Stable Rc



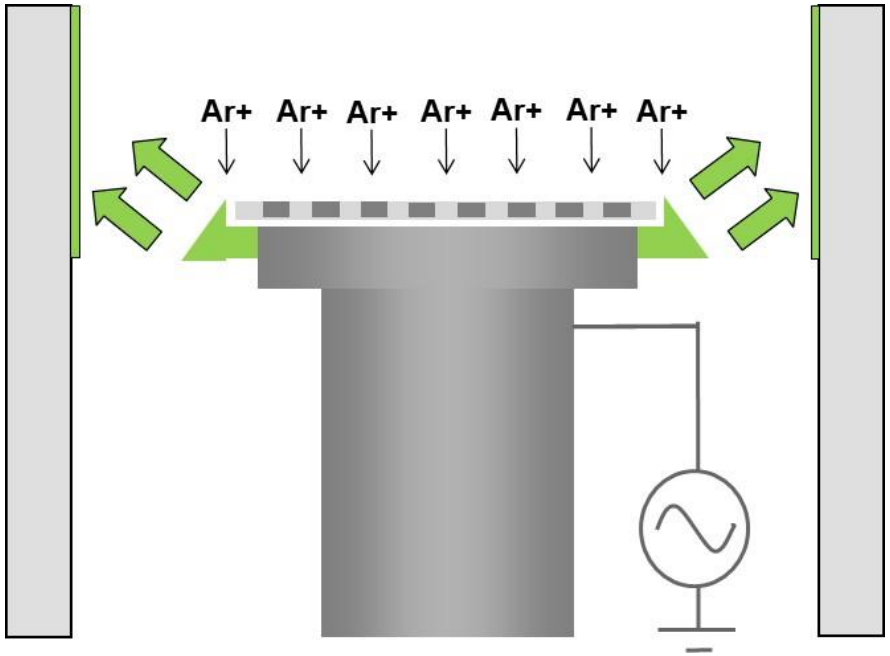


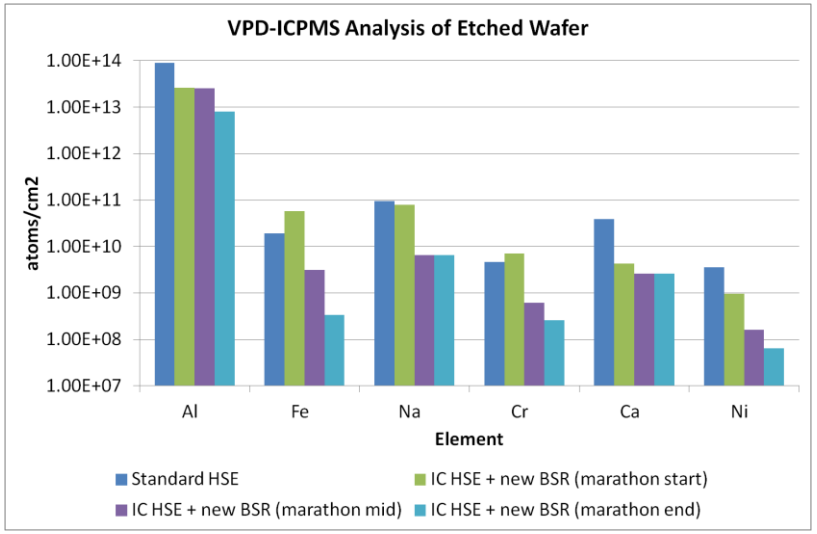
- If not controlled, CO pp will rise during batch
  - Time to pump away >> process time per wafer
  - Result: Rc rises through batch
- In SE-LTX, Rc stays in control – CO pp not rising

Co-Pasting Advantage

- In-situ pasting keeps contamination in check
- Reduces requirement for wafer-based pasting
- Maximise system productivity

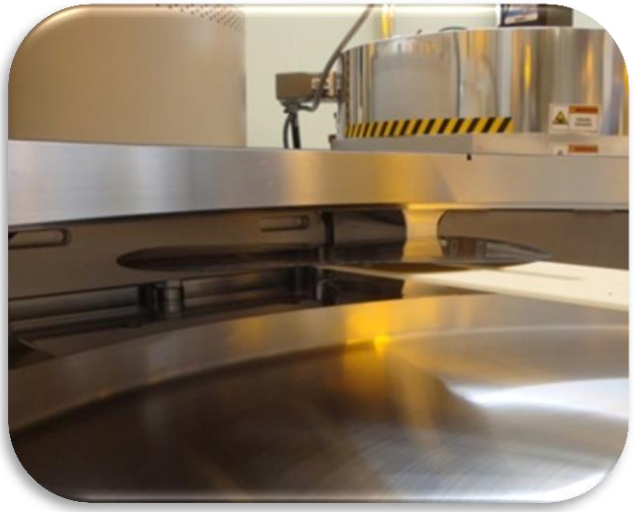
PVD Tool	Wafer Paste Frequency (wafers)
Competitor A	15
Competitor B	25
SPTS	500



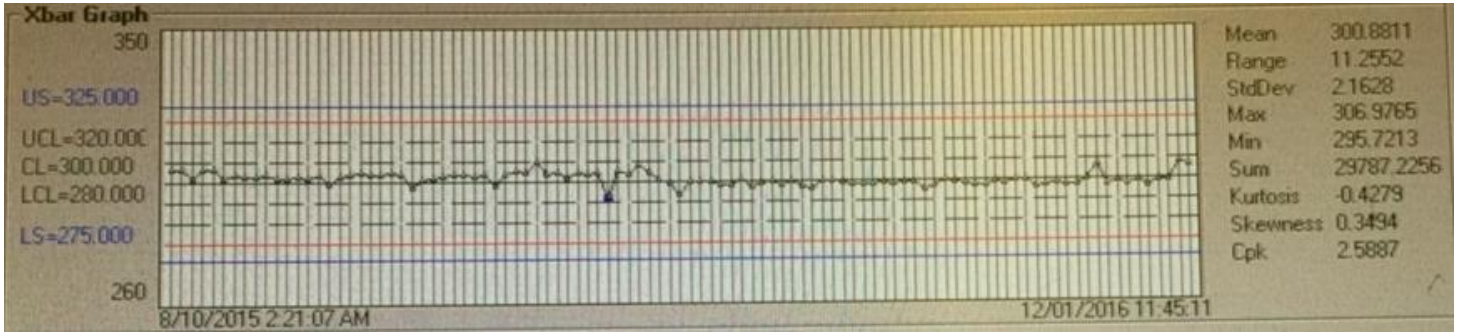


Handling Warped Wafers

- A challenge for FOWLP
- Modifications for thin wafers:-
  - Chamber furniture clearances
  - Robot velocity profiles
  - Wafer lift velocity profiles
  - Slot pitches
  - Temperature rise & fall rates
- Ability to cope with…
  - Thickness ~800 µm, trending < 400 µm
  - Warpage ~3 mm, trending > 6 mm
- Sigma *f*xP designed for > 6 mm bow



Production Validation



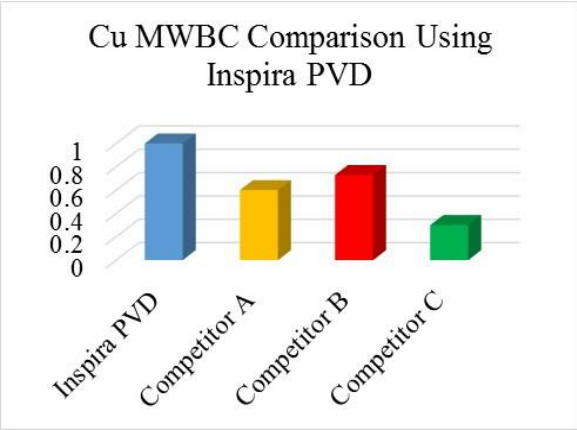
PVD TiW stability over ~30K wfrs

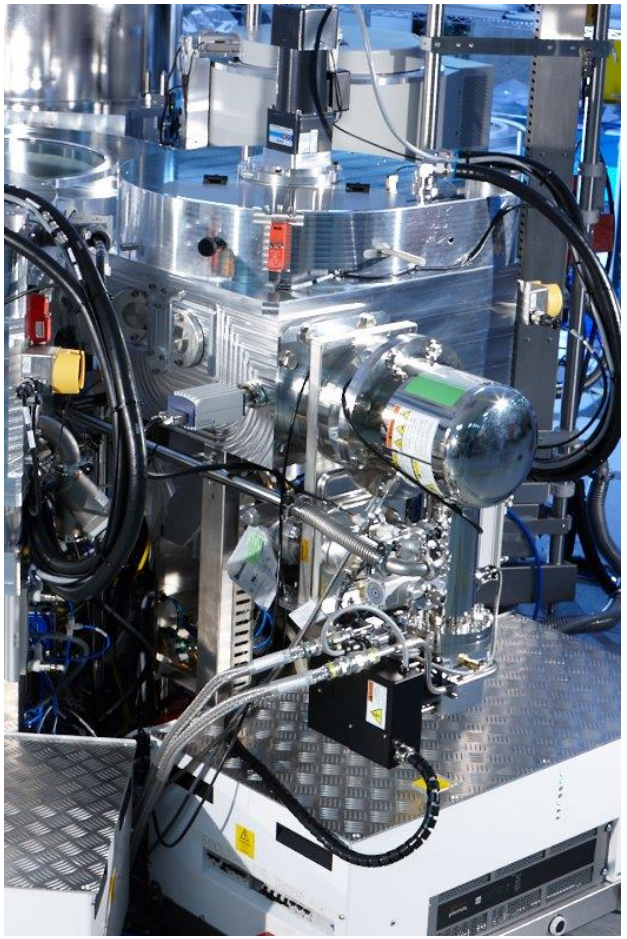
	Mth 1		Mth 2		Mth 3	
Internal ID	Uptime	Util of uptime	Uptime	Util of uptime	Uptime	Util of uptime
Sigma #23	89%	89%	88%	90%	90%	88%
Sigma #25	90%	86%	92%	91%	90%	92%
Sigma #26	91%	90%	91%	89%	92%	90%
Sigma #82	Install to qual		88%	75%	92%	85%

- OSAT started FOWLP production in 2009
  - >1M wafers processed, 200, 300 & larger
  - 1 to 3 LM
- Substrates carrying large & small die (MCM) have largest warpage
  - Average 3 mm with occasional 7-8 mm
- Breakage rates <1 in 30,000. >95% yield

Inspira PVD

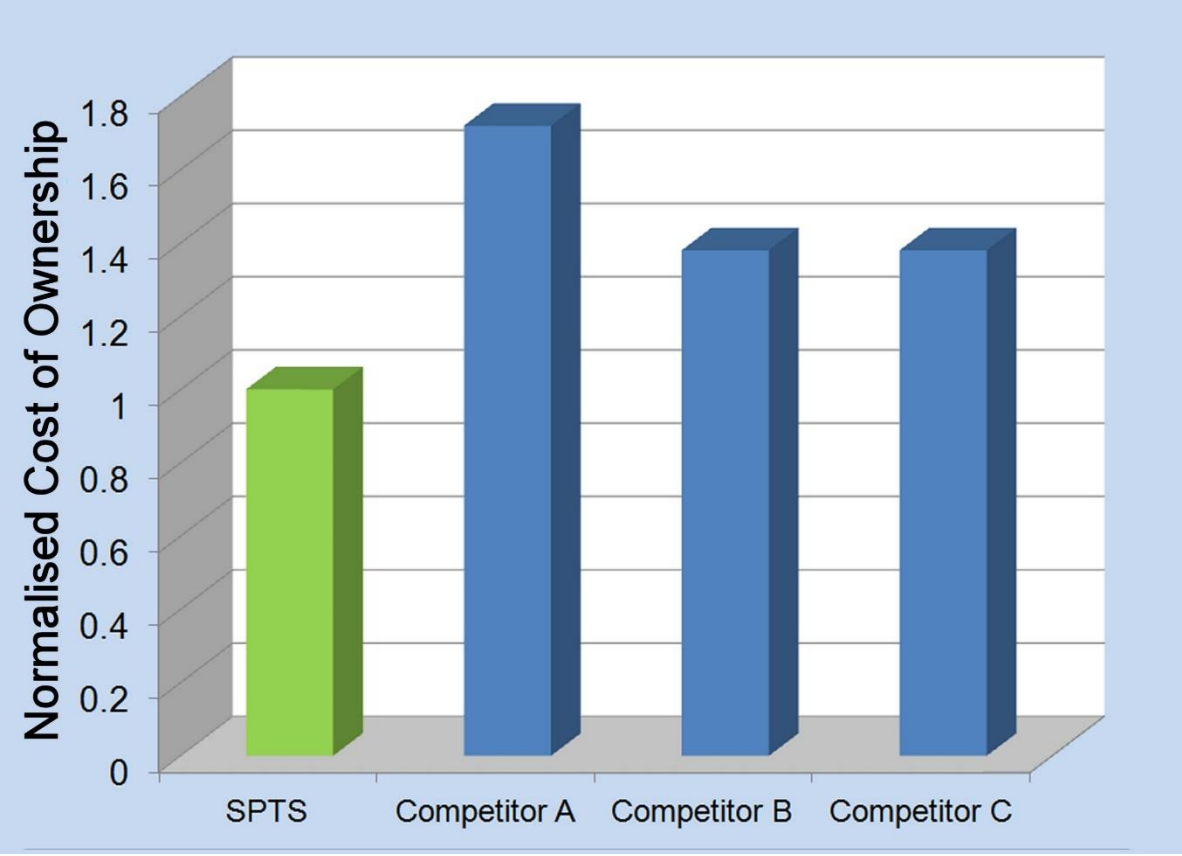
- Designed specifically for BEOL Processing
- Conventional PVD
- On-Board Target PSU
- 2 gas lines
- Heated Platen
- Standard Shielding
  - Shadow Shield Option
- Cryopump Vacuum
- Long Life Targets





Result? The Lowest CoO PVD System

- MWD, Long-Life Pre-Clean, Inspira PVD
  - > 2x T'put for equivalent Rc performance with LT PI or PBO
  - > 30% CoO savings



Summary

- FOWLP is the fastest growing packaging format
  - High density and cost benefits
  - 5-10 µm L/S in production, 2 µm capability proven
- Multiple challenges for PVD vendor
  - Contamination can compromise Rc
  - Particles from re-deposited organics
  - Large Cu exposed area impacts conventional ICP designs
  - Warpage
- Simply adapting existing systems not sufficient
- Solutions required new thinking, validated in production
  - Low Rc at high throughput
  - High uptime from long life SE-LTX with in-situ pasting
  - Low wafer breakage