Fan-Out Wafer Level Packaging (FOWLP) Enables Future IoT Requirements

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ADVANCEMENTS IN BOTH HARDware and software solutions over the past couple of decades have manifested in the emergence of Internet of Things (IoT) era. We are at a juncture when the intersection of a human's world and networks of smart devices capable of sensing, communicating and controlling applications are changing the world we used to know.

A successful IoT ecosystem is constructed by an interconnection of multiple technology platforms, each playing a critical role to harvest, transmit, post-process and store data from the surrounding environments. Sophisticated sensors and chips are embedded in the physical "Things", creating a digital wrap around them in many places such as production lines, buildings, hospitals, solar power plants, etc. However, this fascinating technology stack will not successfully reach its full potential and meet its ambitious goals unless the "Things", in the canvas of an IoT ecosystem, can capture relevant data accurately and securely. Every "Thing" such as a smart watch or smart thermostat is equipped with special solutions which enables them to collect and transmit data while carrying on with their standard function. The IoT solutions are typically a combination of smart hardware (in discrete or as a module) and software platforms (Software Applications, Cloud, and Big Data).

It is expected that IoT proliferation across all industries will accelerate in the next few years to reach beyond 200 billion connected devices by 2020 [1]. This will create and build new markets such as the wearables, but will also reinvent some of the established markets such as healthcare, energy, automotive and consumer. The history of the industrialized world shows that established market segments are often slow to adopt any new technology and innovation. History has also shown that these segments only adopt the technologies which can quickly and seamlessly weave themselves into the fabric of everyday life.

Today, the packaging industry is facing a strong demand to offer smaller footprint and thinner profile CMOS and sensor solutions driven by mobile and IoT proliferation. Even though the existing package technologies continue to be reinvented to meet future requirements, the rise of disruptive packaging solutions is inevitable due to two main reasons:

1. **Thinner Profile**: Although initially driven by the mobile market, the advanced processes such as bare die solutions, compression mold or thinner laminates have established a reduction path. This path will offer advantages to newly established IoT market segments aimed at more than 50% thinner profile which cannot be met by standard assembly approaches.
2. **Chipset Integration**: Each IoT chipset includes multiple sensors, microcontrollers (MCUs) and wireless communication radios. Today, a majority of the chipsets are assembled in discrete solutions. However, the integration of all or a large subset of the chipset into a single module offers the ability to improve the performance (lower leakage, less heat dissipation, etc.), reduce cost and footprint. Therefore, System-in-Package (SiP) solutions are being aggressively pursued by IoT solution providers.

Fan-out wafer level packaging (FOWLP) is among the advanced solutions which have proven to be quite capable of meeting IoT packaging trends for both discrete and SiP device types. Figure 1 shows this technology can integrate multiple dies in a very thin profile molded package with side-by-side integration of devices such as MCUs, radios and encapsulated sensors (for example inertial combos or fingerprint sensors).

FOWLP also offers stacked solutions such as 1.5 sides or 2.5D eWLB-PoP for devices sensitive to molding process or required to directly interface with the environment such as pressure or humidity sensors. In this package type, the bottom eWLB package connects the top solder balls to bottom I/Os by though-vias either directly (one to one connection) or top side redistribution layer (equivalent to a 2.5D package type). The wafer level

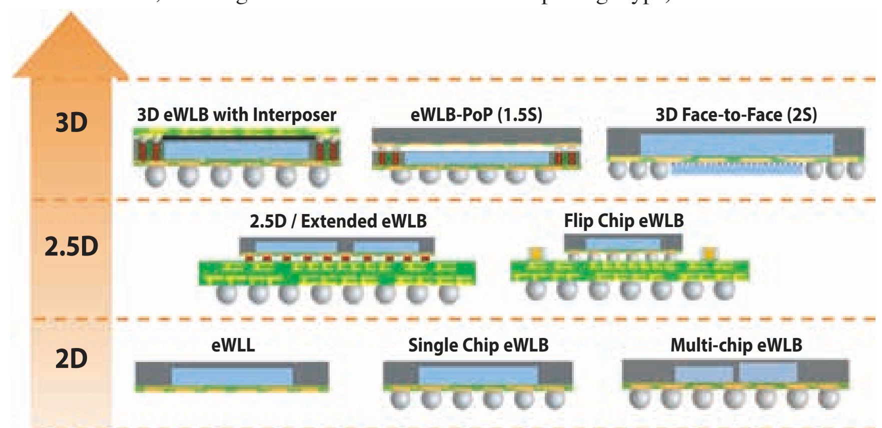

Figure 1: FOWLP (eWLB) package portfolio for wide range of multiple dies, stacked or side-by-side.

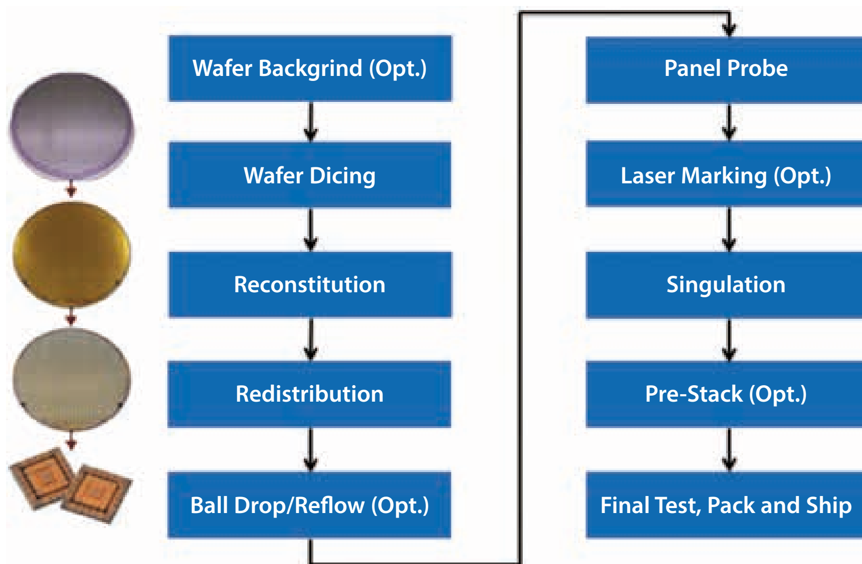

Figure 2: FOWLP (eWLB) process flow. (Opt., i.e. Optional, is applied if required)

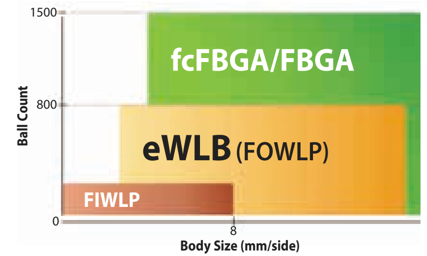

Figure 3: FOWLP (eWLB) sweet-spot covers the common body size and ball count required by IoT SiP solutions.

assembly process (Figure 2) and redistribution of copper traces eliminate the need for a laminate which reduces the package thickness and improves the warpage.

Elimination of the laminate component also results in lower unit cost and simplifies the supply chain and inventory management. In addition, smaller footprint packages may require passive components such as capacitors and inductors to improve sensor performance and eliminate noise fidelity. The FOWLP reconstitution process can be adjusted to embed passives in the package and integrate into the circuit redistribution. It can also meet component level reliability (CLR) of JEDEC MSL1 and temperature cycling range of -55˚C to 125˚C, board level reliability (BLR) of -40˚C to 125˚C temperature cycling and JEDEC standard bend and drop test. Therefore, the package will be a great fit for new and established IoT applications such as consumer, healthcare, automotive and the wearables. The typical body size “sweet spot” for FOWLP (eWLB) ranges from 2~14mm/side and up to 800 pin counts. (Figure 3)

The smaller body sizes (5mm/side or less) are typically a good fit for sensor devices such as health monitoring and environmental sensors. Since sensor devices typically require at least a two-chip solution (ASIC and MEMS/sensing silicon), advanced FOWLP stack-up solutions can enable a very small pitch land-grid array (LGA) and ball-grid array (BGA) eWLB-PoP footprint at a competitive cost vs. the incumbent wirebond solutions. (Figure 4)

The package architecture enables routing on both sides of the package by embedding a direct via across the top to pad side of the package. The top MEMS device is bumped through standard lead-free wafer processing, singulated and assembled by pick-and-place and reflow on the ASIC in the eWLB bottom package. This assembly will eliminate the need for die attach material, assembly wires, protective glob-top and also the typical metal cap or molded package with access cavity, removing the typical laminate or leadframe for routing. Therefore, inverted 1.5S FOWLP offers a much smaller footprint, simplified bill of material (BOM), assembled with a cost competitive panel-level manufacturing process.

The integration of IoT into the fabric of our daily lives and the translation of its data to information and virtual knowledge will soon become the cornerstone of any decision making process. Therefore, the hardware system solution providers are facing an immense task to address the challenge of designing cost effective platforms with often complex sensing capabilities and continuously improving performance requirements. Therefore, a partnership with semiconductor packaging providers is extremely critical to develop disruptive solutions for new and emerging IoT sensors that unlock new frontiers in data acquisition. ◆

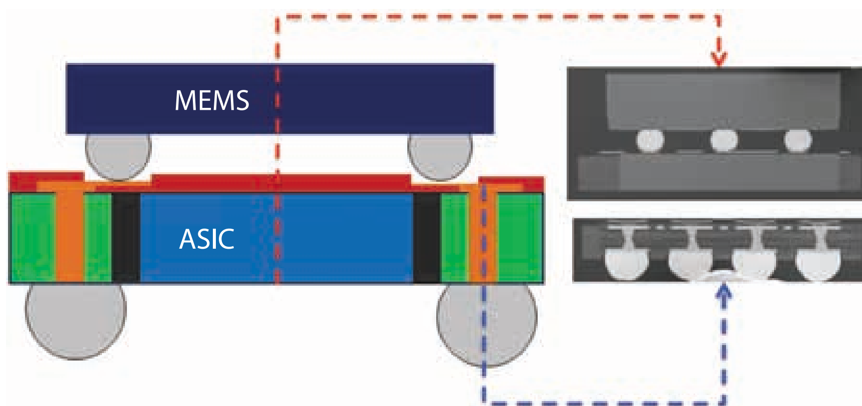

Figure 4: Inverted 1.5S eWLB-PoP (FOWLP) offers significant footprint reduction by stacking ASIC and MEMS.

Reference

1. http://www.zdnet.com/article/internet-of-things-8-9-trillion-market-in-2020-212-billion-connected-things/

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