Effective Post-TSV-DRIE Wet Clean Process for Through Silicon Via Applications

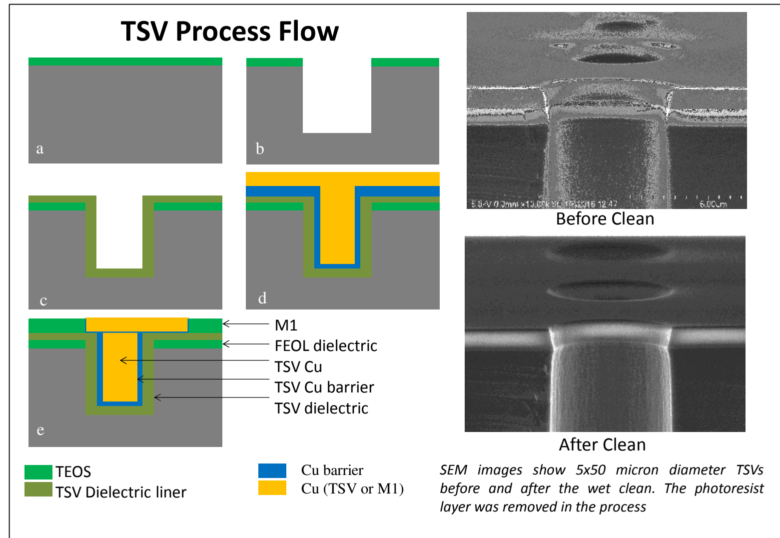
Veeco

Laura Mauer, John Taddei, John Clark, Kenji Nulman
Veeco Precision Surface Processing - Horsham, PA 19044
lmauer@veeco.com

SUNY POLYTECHNIC INSTITUTE

Stephen Olson, Victor Vartanian, Michael Hatzistergos
SUNY Polytechnic Institute - Albany, NY 12203
solson@sunypoly.edu

TSV Process Flow



SEM images show 5x50 micron diameter TSVs before and after the wet clean. The photoresist layer was removed in the process

TSV Process Flow at CNSE for 5x50 and 2x40µm Through Silicon Vias

- (a) TEOS layer
- (b) Photoresist patterning using MUV lithography
- (b) BOSCH-type DRIE to etch silicon
- Cleaning process
- (c) Oxide liner (Ozone/TEOS) by CVD deposition
- (d) Cu barrier and seed layers deposited followed by Cu plating
- (e) CMP to remove overburden followed by M1 processing

The CNSE POR Cleaning process uses an oxygen ash as part of the RIE process, followed by dilute HF and $NH_4OH:H_2O_2:H_2O$ to remove photoresist and the sidewall polymer.

TSV Clean Split Table

		Number of Wafers			
		5x50		2x40	
Soak Time (s)	Rinse	Ash	No Ash	Ash	No Ash
1800	Mega DIW	3	3	3	3
	SC1	3	2	-	3
2700	Mega DIW	3	1	-	-
	SC1	3	2	-	-
3600	Mega DIW	3	3	3	3
	SC1	3	3	3	2
POR		5	3	6	3
No Clean		2	2	-	-

POR	*Replace Existing Clean Only*	*Replace Ash and Existing Clean*
Pattern TSVs	Pattern TSVs	Pattern TSVs
RIE Oxide and Si	RIE Oxide and Si	RIE Oxide and Si
Ash	Ash	
DHF, SC1 clean	Veeco Wet Clean	Veeco Wet Clean
Dielectric Liner	Dielectric Liner	Dielectric Liner
		33% reduction in RIE Process Time

Veeco Clean Process Sequence in WaferStorm®

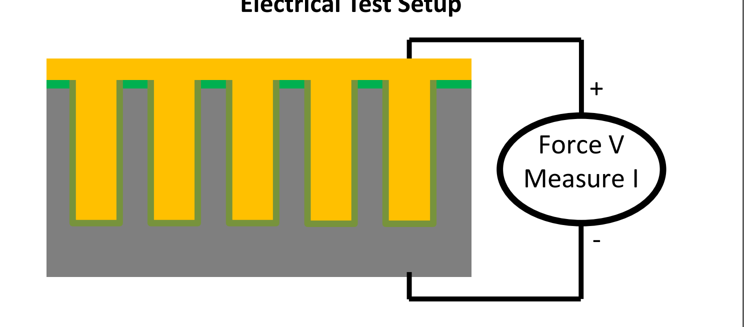
Veeco Wet Clean Process:

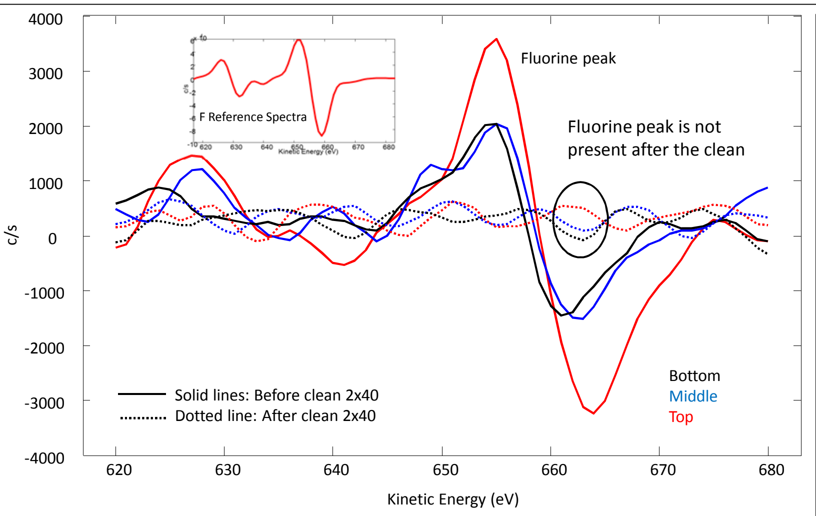
- Immersion batch soak in Dynastrip™ DL9150
- Single wafer high pressure fan spray with Dynastrip™ DL9150
- Rinse and spin dry

Eliminates need for oxygen ash process to strip photoresist

Electrical test was used to evaluate the performance of the cleaning process. Arrays of TSVs are connected to bond pads on the front surface of the wafer. Voltage is applied and leakage current is measured to the substrate. Voltage is then ramped in step pattern to determine voltage where TSV dielectric breakdown occurs.

Electrical Test Setup





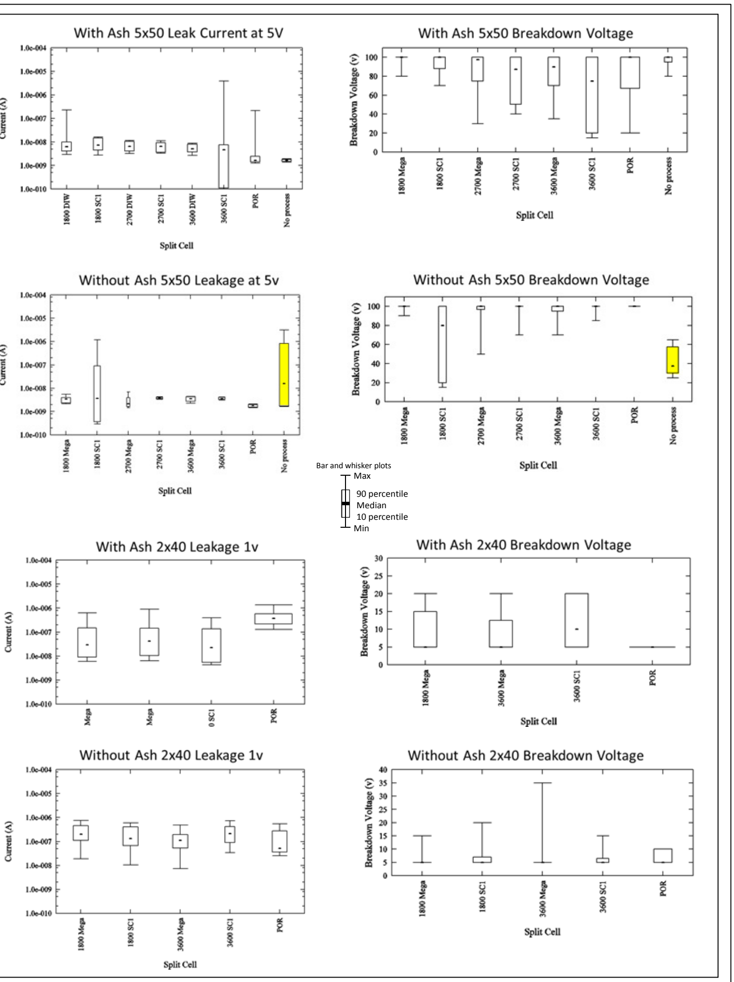
Results discussion

Auger Electron Spectroscopy was used to examine the 2x40 µm TSV sidewalls before and after cleaning. Data are shown for the 1800 second soak/SC1 rinse process split. Three locations inside the TSV were measured (top, middle, bottom). Background levels were obtained from freshly cleaved silicon next to the TSV ("off TSV").

Electrical test was done on 32 dies per wafer. Veeco wet clean had average leakage current approximately the same as POR. The split cell "no clean" wafers (without a wet clean) performed similarly to POR for the wafers with the Ash process. Without the Ash process the results are quite different indicating the sidewall polymer is removed primarily by the Ash in the POR. For the Veeco wet clean there is no difference without Ash.

		Concentration (atomic %)							
		Si		O		C		F	
		B	A	B	A	B	A	B	A
5X50	**Top**	41	59	31	29	28	12	1	-
Before Clean	**Middle**	43	60	35	29	22	12	0.5	-
After Clean	**Bottom**	44	60	37	28	19	12	-	-
	Off TSV	51	73	28	18	22	9	-	-
2X40	**Top**	28	41	2	23	69	37	2	-
Before Clean	**Middle**	33	45	3.5	24	63	31	1	-
After Clean	**Bottom**	37	60	4	24	59	17	1	-
	Off TSV	79	68	16	19	5	14	-	-

Auger analysis shows the carbon and fluorine concentrations on the TSV sidewall decreases after cleaning. (B=before cleaning; A=after cleaning)



Conclusions

- Electrical and physical analysis shows the Veeco wet clean removes both the photoresist and sidewall polymer residues from the TSVs.
- The new clean process can replace the ash, reducing the TSV RIE process time by 33%.

Acknowledgements: *Kim Pollard and Diane Scheele (Dynaloy) for technical support and guidance using Dynastrip™ for TSV Clean. John Mucci (CNSE) for assistance in developing TSV Etch recipes for this work.*