

Our Early and Ongoing Work in 3D Integration

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**Corresponding Author*



Dr. Peter Ramm

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3D History at Fraunhofer Munich

A Selection of Large Projects on 3D Integration (1)

1987 – 1989: German Research Project (BMFT)

Siemens, AEG, Philips, Fraunhofer IFT Munich

„Three-dimensional Integrated Circuits – 3D“

→ 3D CMOS Devices Based on Si Recrystallization for **3D-ICs**

SIEMENS

 IFT
Fraunhofer Institut Festkörpertechnologie

1993 – 1996: German Research Project (BMBF)

Siemens and Fraunhofer IFT Munich

„Cubic Integration - VIC“

→ TSV Technology for **3D-SICs**

SIEMENS

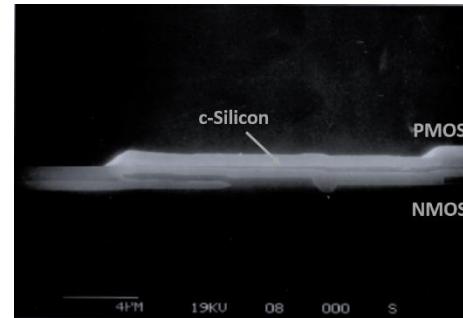
 IFT
Fraunhofer Institut Festkörpertechnologie

3D Integration – Definitions (ITRS)

- 3D-IC

3D Integrated Circuit: stacking of transistor layers
(3D connections at density level of local interconnects)

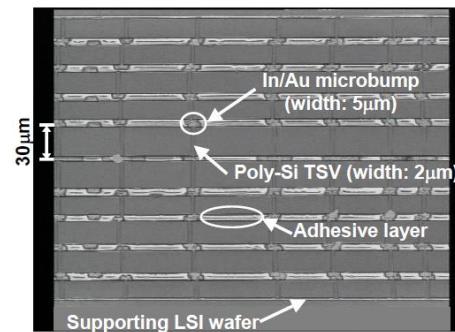
Source: Fraunhofer



- 3D-SIC

3D Stacked Integrated Circuit
(very high TSV densities)

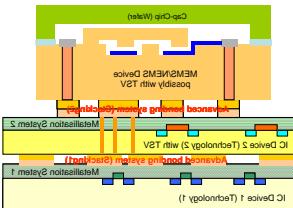
Source: Tohoku University



- 3D-SOC

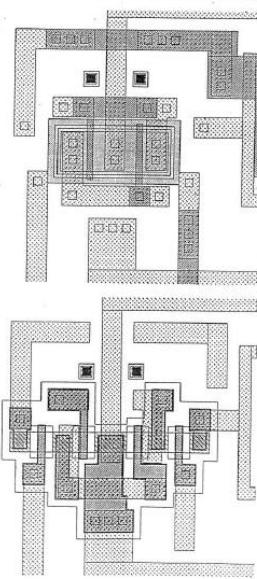
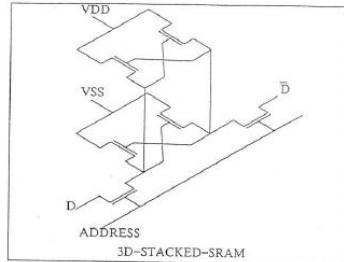
3D System-On-Chip: stacking of devices or large IC blocks (global level)

➤ **Fabrication of Heterogeneous Systems**

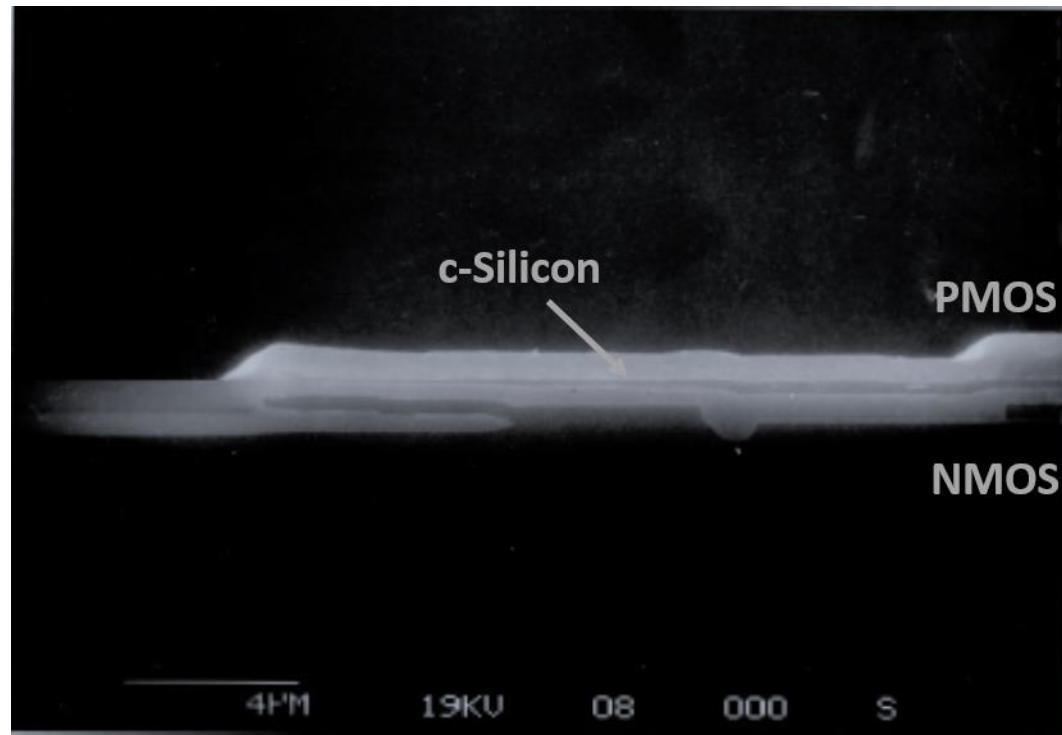


Source: Fraunhofer

1987 – 1989: German Research Project (BMFT) Siemens, AEG, Philips, Fraunhofer IFT Munich „Three-dimensional Integrated Circuits – 3D“



3D SRAM Cell Layout



3D CMOS Devices - Based on Recrystallization
of Thin Si (Excimer Laser)

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„Cubic Integration - VIC“

→ TSV Technology for 3D-SICs



Early paper on complete 3D-TSV process flow

MICROELECTRONIC ENGINEERING

An International Journal of Semiconductor Manufacturing Technology

SIEMENS


Fraunhofer IFT
Institut
Festkörpertechnologie

**Munich's
3D Team
in the 90's**

Microelectronic Engineering 37/38 (1997) 39–47

Three dimensional metallization for vertically integrated circuits (Invited lecture)

P. Ramm^{a,*}, D. Bollmann^a, R. Braun^a, R. Buchner^a, U. Cao-Minh^a, M. Engelhardt^b,
G. Errmann^a, T. Graßl^a, K. Hieber^a, H. Hübner^b, G. Kawala^a, M. Kleiner^b, A. Klumpp^a,
S. Kühn^b, C. Landesberger^a, H. Lezec^c, W. Muth^a, W. Pamler^b, R. Popp^a, E. Renner^b,
G. Ruhl^a, A. Sänger^b, U. Scheler^b, A. Schertel^c, C. Schmidt^b, S. Schwarzl^b, J. Weber^a,
W. Weber^b

^aFraunhofer Institute for Solid State Technology, Hansastr. 27d, D-80686 München, Germany

^bSiemens AG, Corporate Technology, Microelectronics, Otto-Hahn-Ring 6, D-81739 München, Germany

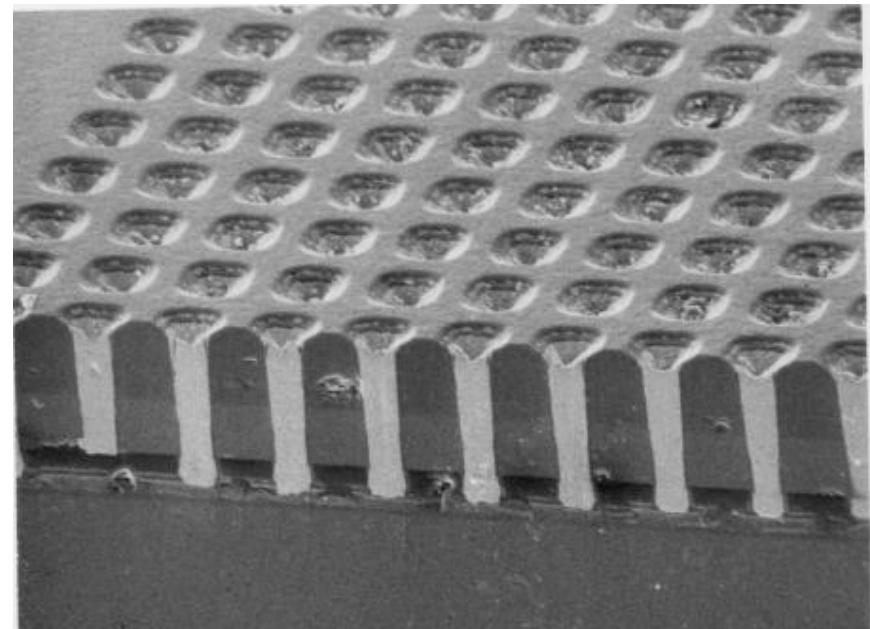
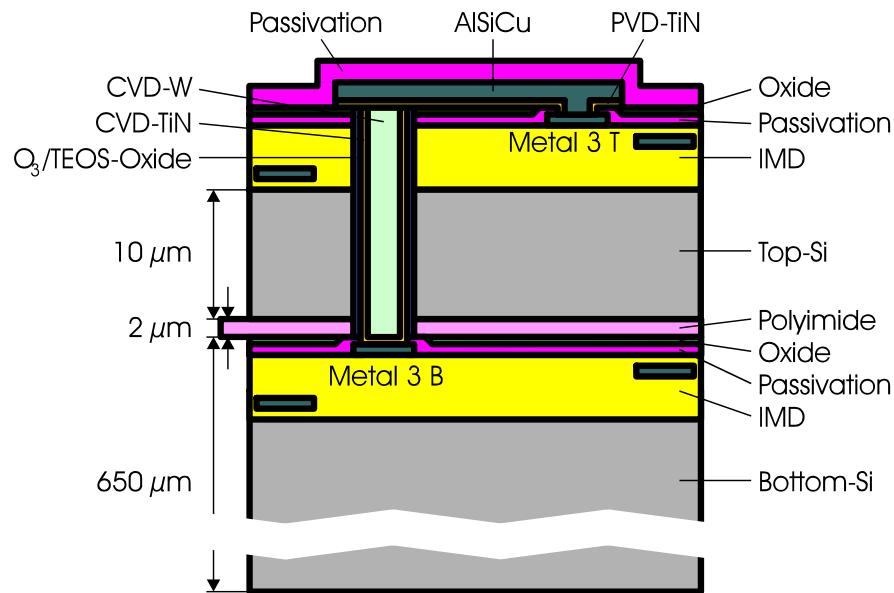
^cMicrion Europe GmbH Garmischer Str. 4, D-80339 München, Germany

Early 3D-SiC Concept: „InterChip-Via“ ICV Technology

Key Persons in Process Development:

**Manfred Engelhardt, Werner Pamler, Annette Sänger, Siegfried Schwarzl
Reinhold Buchner, Armin Klumpp, Günther Ruhl, Josef Weber, Peter Ramm**

SIEMENS
Fraunhofer IFT
Institut
Festkörpertechnologie





Ramm
BV

1995

FIRST
INTERNATIONAL
DIELECTRICS
& **CMP** FOR VLSI/ULSI
MULTILEVEL
INTERCONNECTION
CONFERENCE,
SHORT COURSE
AND
EXHIBITION

February 20 - 22, 1995

SANTA CLARA MARRIOTT HOTEL
Santa Clara, CA.

HIGHLIGHTS:

- New Developments in C.M.P. Processes for ULSI—
(See Sessions V and X, plus Short Course)
- "Industry Methodologies for the Low Dielectric Challenge"---
Dr. Thomas Seidel, SEMATECH
Keynote Address
- "C.M.P. - The Global Planarity Tour"---
Michael A. Martincz, SEMI
Short Course Luncheon
- "Challenges of the National Technology Roadmap for Semiconductors"---
Dr. David Fraser, INTEL
DUMIC Luncheon
- SHORT COURSE on DIELECTRICS for ULSI MULTILEVEL INTERCONNECTION**---
Monday, February 20, 1995
- DUMIC includes over 50 papers and almost 200 authors from 48 different companies/universities/agencies in 7 different countries from around the world.---

DEPOSITION OF TEOS/O₃ OXIDE LAYERS FOR APPLICATION IN VERTICALLY INTEGRATED CIRCUITS TECHNOLOGY

T. Graßl and P. Ramm

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M. Engelhardt

Siemens AG, Corporate Research and Development; 81730 Munich; Germany

Z. Gabrić and O. Spindler

Siemens AG, Semiconductors Technology Processes, Equipment, Support;
81730 Munich; Germany

Abstract

Chemical vapour deposited oxide with TEOS/O₃ chemistry is applied as isolating dielectric layer in a three-dimensional metallization technique. The specific CMOS compatible process, we call Inter-Chip-Via technology (ICV), realizes the integration of devices, fabricated with conventional planar technologies, to 3-dimensional micro-electronic systems. The devices are fabricated within different substrates and fitted together after thinning of the top substrate from the backside with a remaining wafer thickness of typically 10 µm. To provide the inter-chip contacts via holes with openings in the range of 2 µm will be etched through the passivation and the inter metal dielectrics of the top device layer and the remaining silicon bulk down to the metal of the bottom device. A TiN/W sandwich structure is used as inter-chip-via metallization between the top chip and the bottom chip metallization. One of the major items of this technology is the dielectric isolation between the tungsten filled vias and the silicon bulk. This could be achieved with a specific modular plasma etch technique, an optimized deposition process and subsequent spacer etch of the TEOS/O₃ oxide layers.

Dr. Peter Ramm

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DUMIC 1995

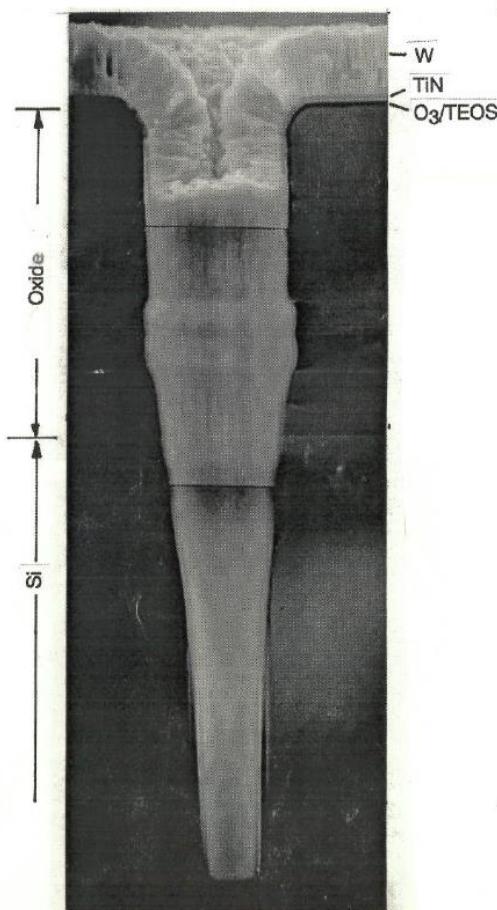
DEPOSITION OF TEOS/O₃ OXIDE LAYERS FOR APPLICATION
VERTICALLY INTEGRATED CIRCUITS TECHNOLOGY

T. Grassl and P. Ramm

Fraunhofer-Institute for Solid State Technology, 80686 Munich, Germany

M. Engelhardt

Siemens AG, Corporate Research and Development, 81730 Munich, Germany



ECTC 2015

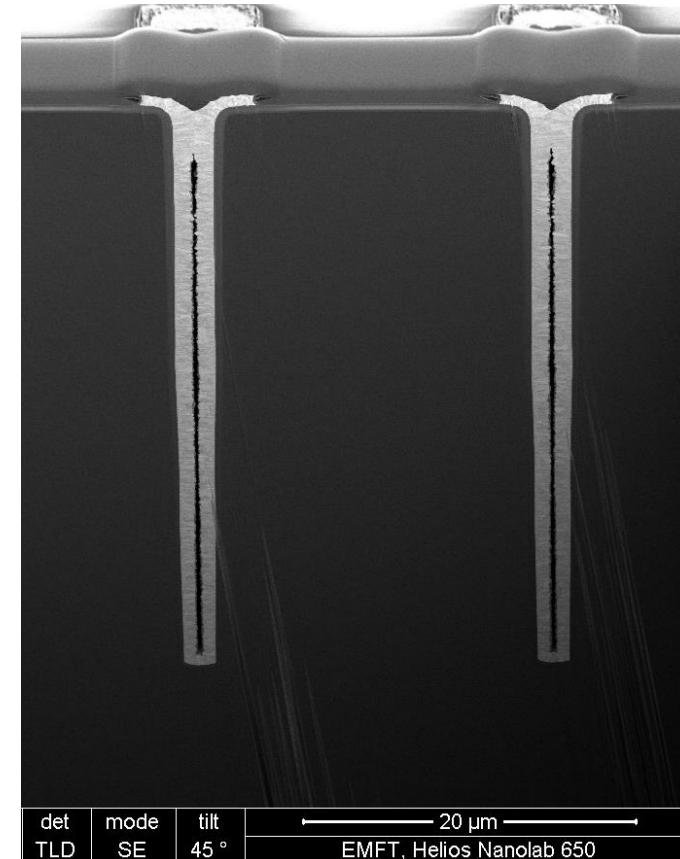
Fine Pitch 3D-TSV Based High Frequency Components for RF MEMS Applications

Wolfgang A. Vitale¹, Montserrat Fernández-Bolaños¹, Reinhard Merkel², Amin Enayati³, Ilja Ocker³, Walter De Raedt³, Josef Weber⁴, Peter Ramm⁵ and Adrian M. Ionescu³

¹NanoLAB, École Polytechnique Fédérale de Lausanne (EPFL)
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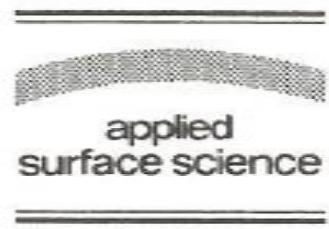
Dr. Peter Ramm

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Early W-TSV



Applied Surface Science 91 (1995) 382–387



Deposition of titanium nitride/tungsten layers for application in vertically integrated circuits technology

G. Ruhl ^{a,*}, B. Fröschle ^a, P. Ramm ^a, A. Intemann ^b, W. Pamler ^c

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^b *Siemens Components Inc./IBM 64 MB dev. group Dep. B12, East Fishkill, NY 12533, USA*

^c *Siemens AG, Corporate Research and Technology, D-81730 Munich, Germany*

Received 20 March 1995; accepted for publication 10 April 1995

CVD of W as the Final Process Step of a Complete Process Flow



10 μm

Process Flow

- Lithography
- Deep Dielectric Trench Etch
- Resist Strip
- CVD of SiO_2
- Spacer 1 Etch
- Deep Silicon Trench Etch
- Via clean
- CVD of SiO_2
- Spacer 2 Etch
- CVD of TiN
- CVD of W

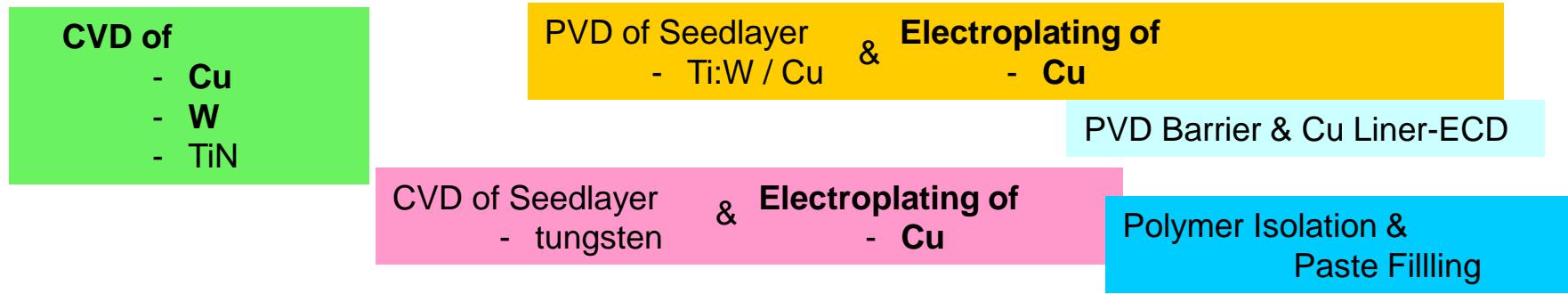
Table INTC8 Intermediate Interconnect Level 3D-SiC Roadmap

Intermediate Level, W2W 3D-stacking	2011-2014	2015-2018
Minimum TSV diameter	1-2 μm	0.8-1.5 μm
Minimum TSV pitch	2-4 μm	1.6-3.0 μm
Minimum TSV depth	6-10 μm	6-10 μm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 μm	0.5-1.0 μm
Minimum contact pitch	2-3 μm	2-3 μm
Number of tiers	2-3	8-16 (DRAM)

TSV Metallization

Source: ITRS 2011 Edition

1.0 μm 3.5 μm 5 μm 10 μm 100 μm TSV Diameter



10 μm 25 μm 70 μm 100 μm TSV Depth
 10:1 5:1 7:1 1:1 Aspect Ratio

electroless Seedlayer & Cu-ECD

Based on: Handbook of 3D Integration, Vol.1
 edited by P. Garrou, C. Bower and P. Ramm

Early proposal for 3D-IC application: Memory on Logic

IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY—PART B, VOL. 19, NO. 4, NOVEMBER 1996

709

Performance Improvement of the Memory Hierarchy of RISC-Systems by Application of 3-D Technology

Michael B. Kleiner, Stefan A. Kühn, Peter Ramm, and Werner Weber

Abstract—In this paper, the performance of the memory hierarchy of RISC-systems for implementations employing three-dimensional (3-D) technology is investigated. Relating to RISC-systems, 3-D technology enables the integration of multiple chip-layers of memory together with the processor in one 3-D IC. In a first step, the second-level cache can be realized in one 3-D IC with processor and first-level cache. This results in a considerable reduction of the hit time of the second-level cache due to decreased access time and a larger allowable bus-width to the second-level cache. In a further step, the main memory can be integrated which relieves restrictions with respect to the bus-width to main memory. The use of 3-D technology for system implementation is observed to have a significant impact on the optimum design and performance of the memory hierarchy. Based on an analytical model, performance improvements on the order of 20% to 25% in terms of the average time per instruction are evaluated for implementations employing 3-D technology over conventional ones. It is concluded that 3-D technology is very attractive for future RISC-system generations.

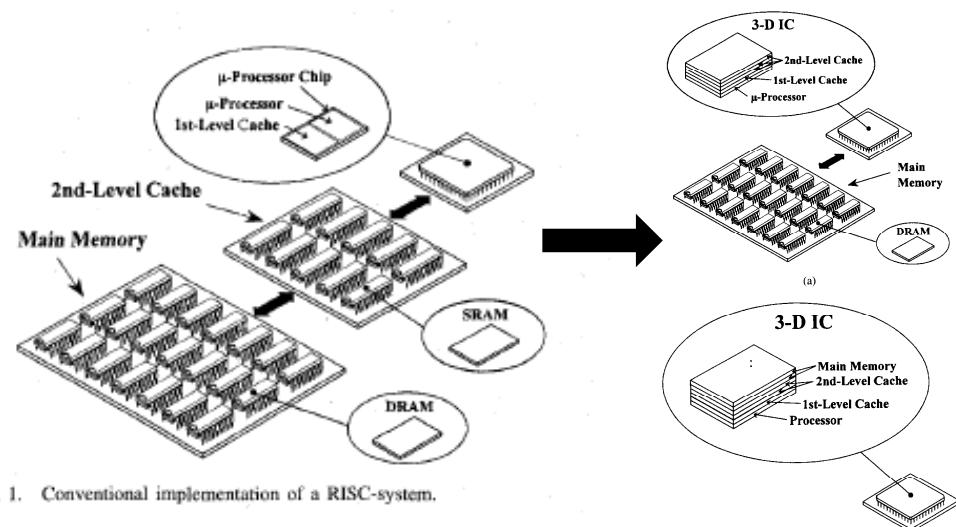


Fig. 1. Conventional implementation of a RISC-system.

Thermal Analysis of Vertically Integrated Circuits

Michael B. Kleiner^{1,2}, Stefan A. Kühn^{1,2}, Peter Ramm³, and Werner Weber¹

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³Fraunhofer Institute for Solid
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Abstract—In this paper, a thermal analysis of Vertically Integrated Circuits (VIC) is presented for the first time. Based on a 1-D model, temperature differences in VICs of less than 10 °C are evaluated for most practical applications. Detailed 3-D investigations show that self-heating of MOSFETs in the upper chip-layers of a VIC is more pronounced than in bulk CMOS and that it strongly depends on the thickness of the silicon remaining in the chip-layer. In addition, thermal coupling between adjacent transistors is observed to be much more marked.

I. INTRODUCTION

Vertically Integrated Circuits (VIC) [1-3] are currently a major research interest. The dramatic increase in packaging

density, the large realizable interconnect density between adjacent chip-layers of more than 100 000/cm², and the possibility to integrate various technologies in one stack make VICs very attractive for a wide range of applications [4]. Fig. 1 illustrates schematically the process sequence for the fabrication of VICs. Individual chip-layers are manufactured using state-of-the-art process technologies. The upper chip-layers are thinned from the reverse side prior to stacking. Vertical interconnects with lateral dimensions on the order of 1 μm are fabricated between adjacent chip-layers.

Thermal aspects, such as excessive overall temperature gradients during operation as well as local heating inside VICs are frequently believed to become a problem or even be a blocking point for such technologies. It is the intent of this work to qualitatively and quantitatively investigate heating in VICs.

3D History at Fraunhofer Munich

A Selection of Large Projects on 3D Integration (2)

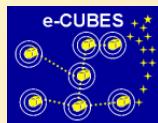
1999 – 2003: German EUREKA Project

Infineon, Giesecke & Devrient, Fraunhofer IZM Munich

„Vertical System Integration“ – VSI®

→ TSV Technology optimized for Die-to-Wafer Stacking of 3D-SOCs

2007 – 2009: European Integrated Project (IST)

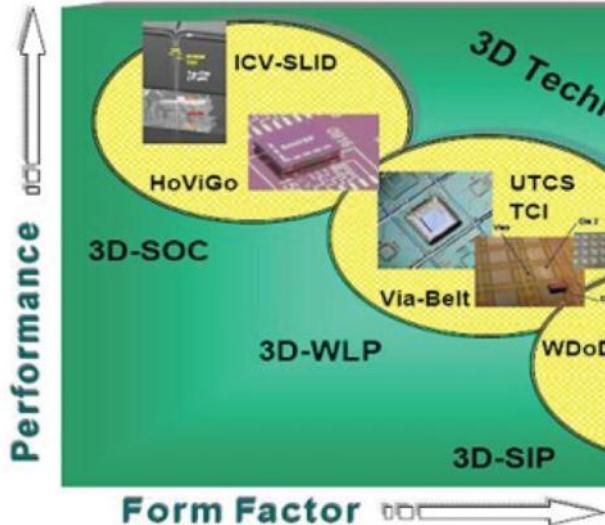
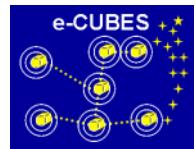


Infineon, Philips, Thales, SensoNor, 3D-PLUS, IMEC, CEA, Fraunhofer, ...

e-CUBES® – 3D-Integrated Wireless Sensor Systems

→ Technology Platform for **3D Heterogeneous Integration**

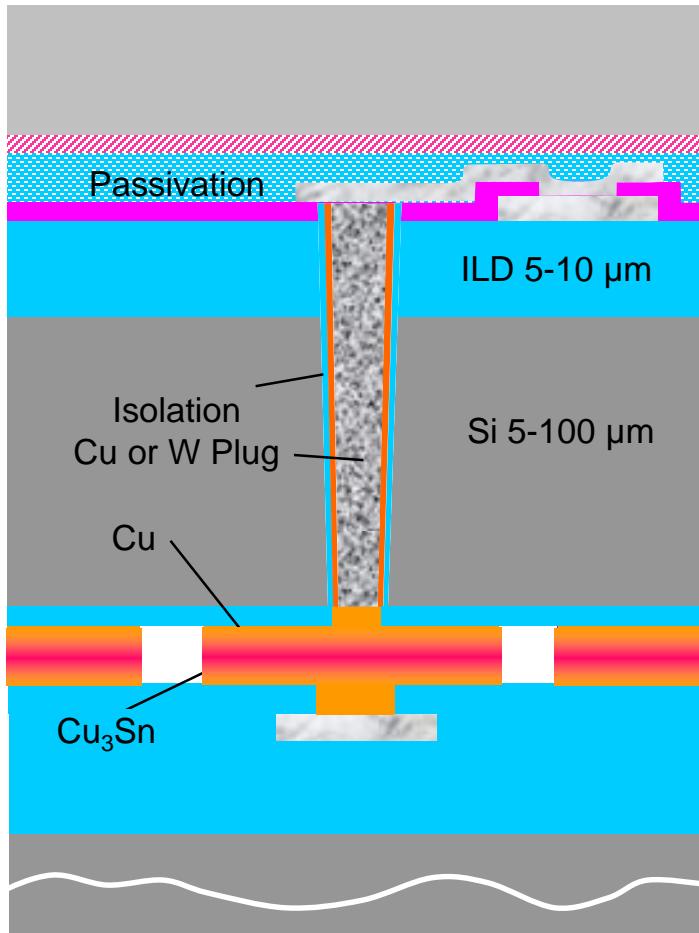
European 3D Technology Platform



Technology	e-CUBES Partner
3D-SOC	
Through Silicon Via (TSV) Technology (ICV-SLID)	Fraunhofer EMFT (formerly IZM-M)
Hollow Via & Gold Stud Bump Bonding (HoViGo)	SINTEF
3D-WLP	
Thin Chip Integration (TCI/UTCS)	Imec and Fraunhofer IZM & EMFT
Via Belt Technology Chip-in-Polymer and µInsert)	CEA-Leti
3D-SIP	
High Performance Package-in-Package Technology (HiPPiP)	3D-PLUS
Wirefree Die-on-Die Technology (WDoD)	3D-PLUS
Submicron Wire Anisotropic Conductive Film Assembly (SW-ACF)	Tyndall

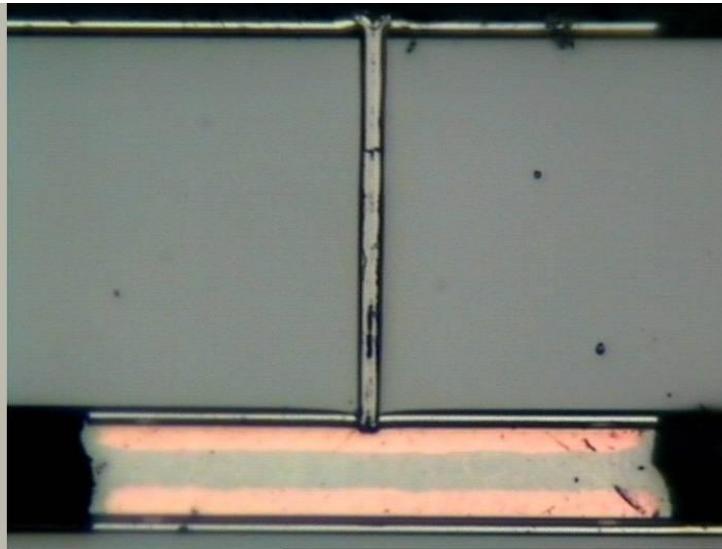
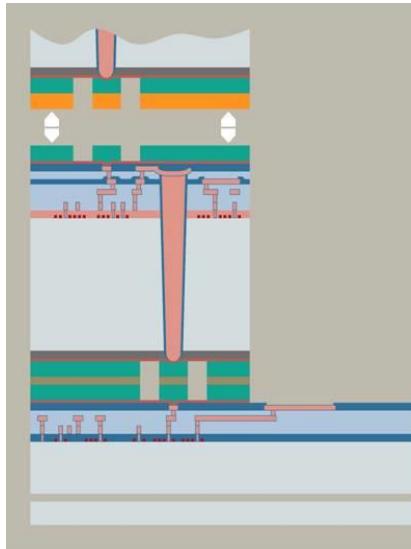
Futue Fab International, Issue 34 (July 2010)
“The European 3D Technology Platform (e-CUBES)”
P. Ramm, A. Klumpp, J. Weber, M. Taklo, N. Lietaer, W. De Raedt, T. Fritzsch,
T. Hilt, P. Couderc, C. Val, A. Mathewson, K. M. Razeeb, F. Stam

Heterogeneous Integration by TSV-SLID Technology (Chip-to-Wafer)



- Fabrication of Tungsten- or Copper-filled TSV on Top Substrate
- Via Opening and Metallization
- Thinning
- Opening of Plugs
- Through Mask Electroplating
- Chip/Wafer Alignment and Bonding

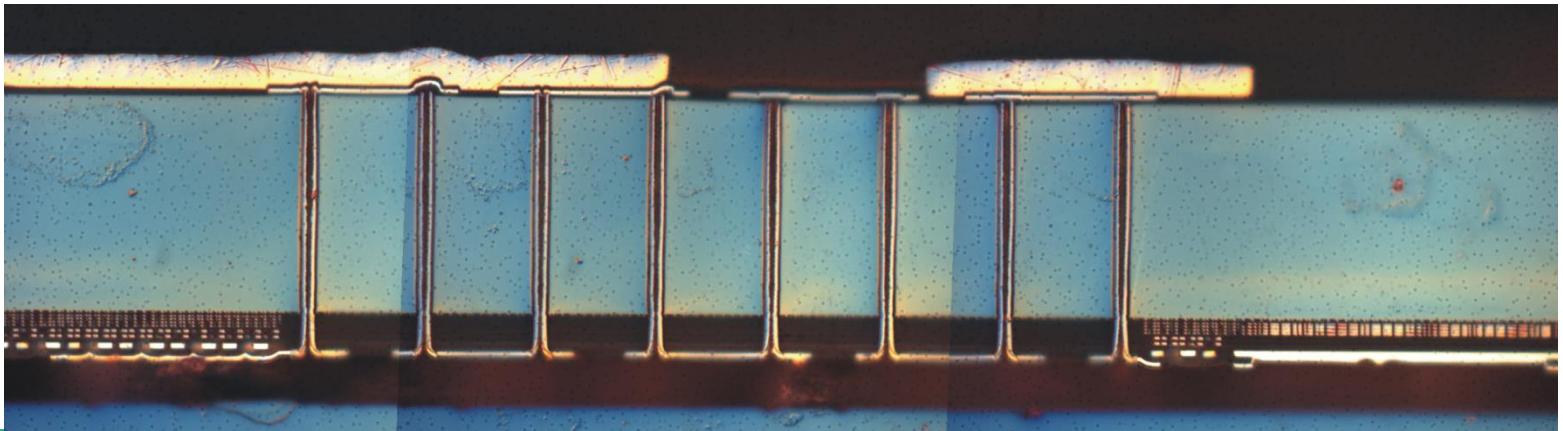
TSV-SLID – a robust 3D TSV Technology



Source: Fraunhofer EMFT

ASIC (7-level metallization)
Process control module
(PCM)

Daisy
chains
in PCM

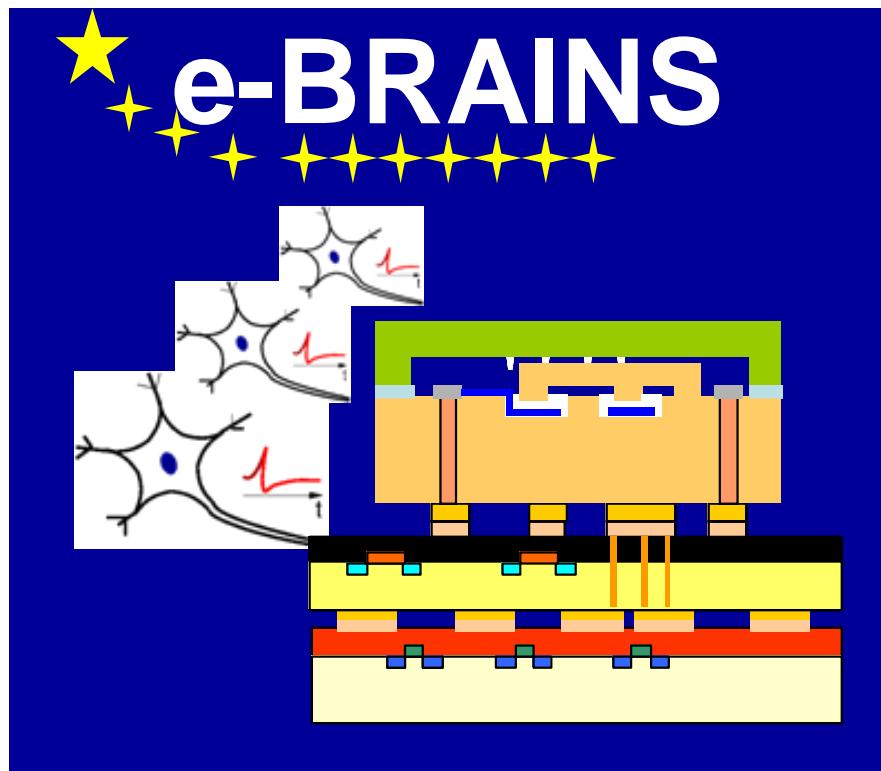


Dr. Peter Ramm

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e-BRAINS: Best-Reliable Ambient Intelligent Nanosensor Systems by Heterogeneous Integration

supported by the European Commission
under support-no. ICT-257488



www.e-brains.org

Dr. Peter Ramm

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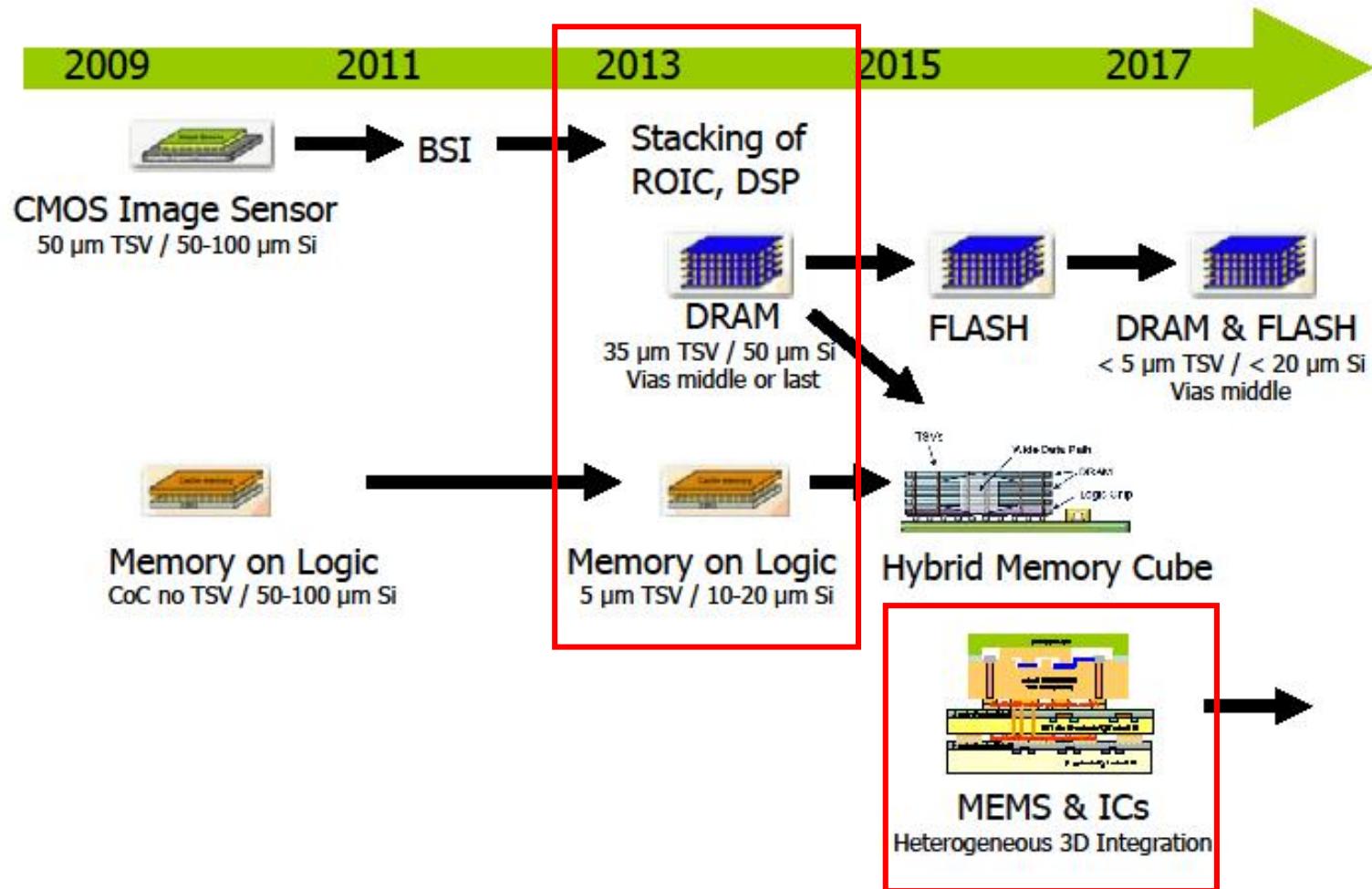
SIEMENS



vermon

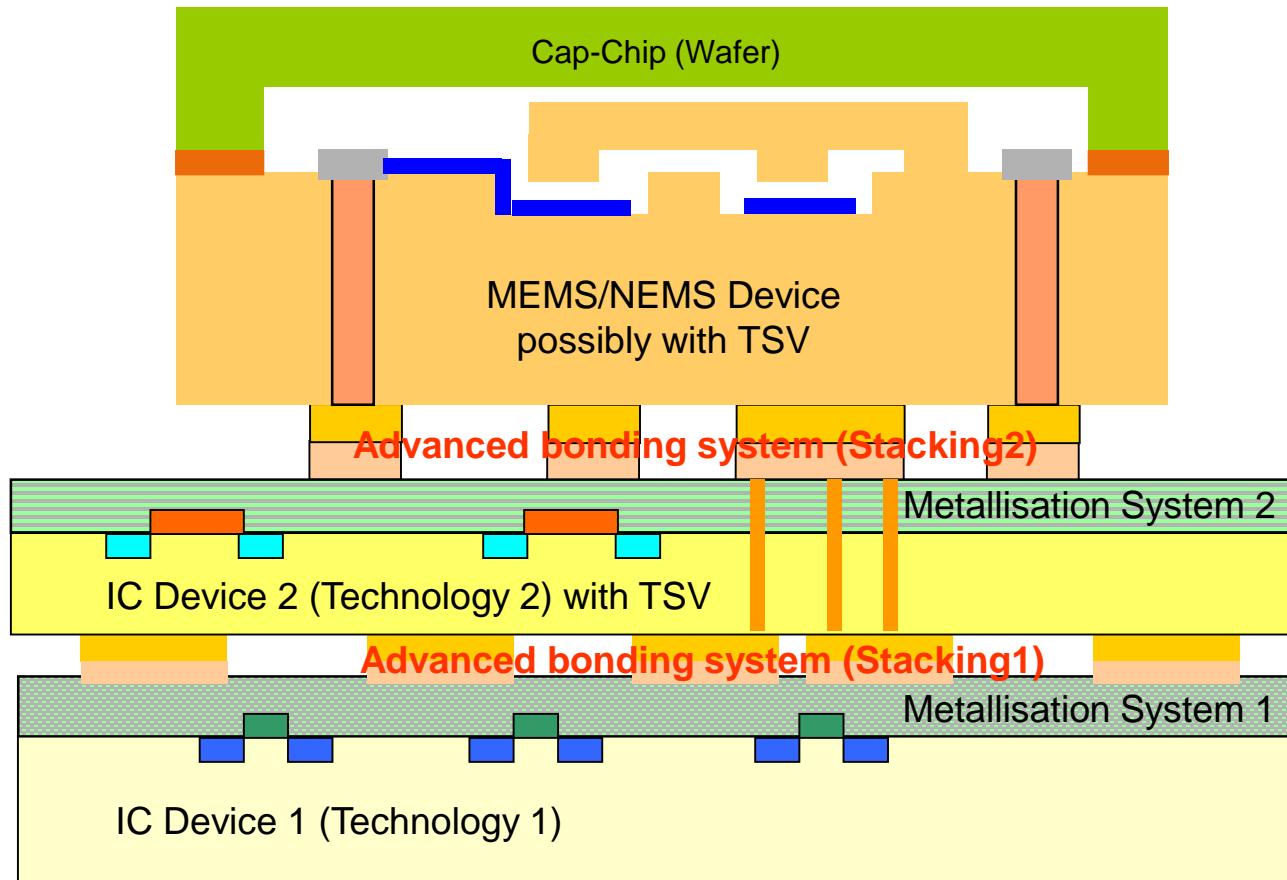


Application Development 3D-ICs



Source: R. Beica, J.-C. Eloy and P. Ramm: „Key Applications and Market Trends for 3D Integration and Interposer Technologies“
in „Handbook of 3D Integration“ Vol. 3, Wiley-VCH (2014)

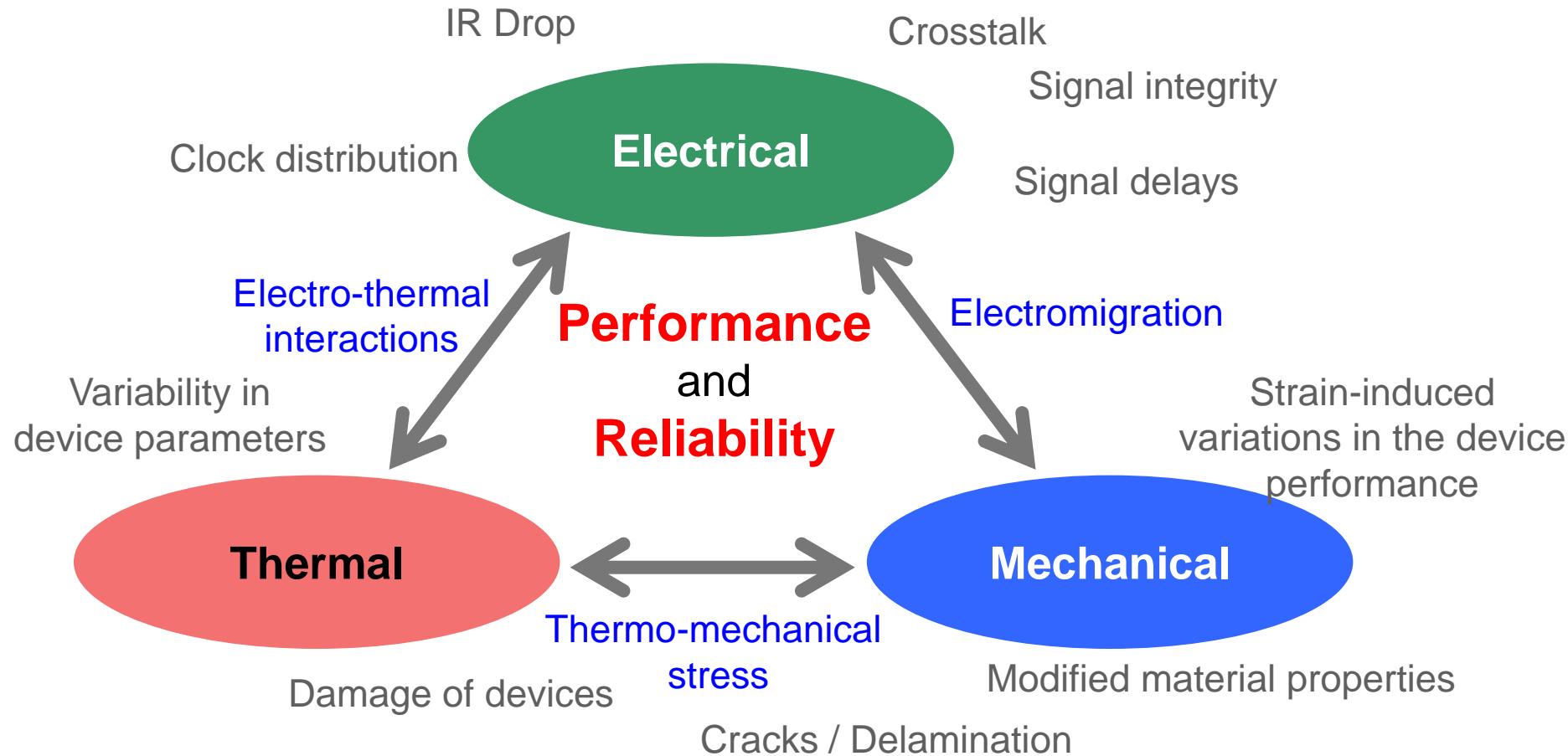
3D MEMS/NEMS & IC Integration – a Challenge!



Issues for **producibility** and **reliability**:

- Fragile mechanical structures in MEMS/NEMS devices
- Stress induced by TSVs and **bonding system** of thin IC devices

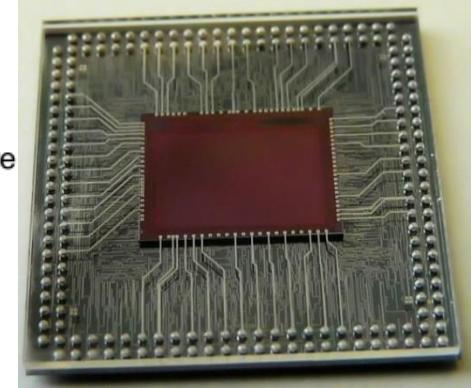
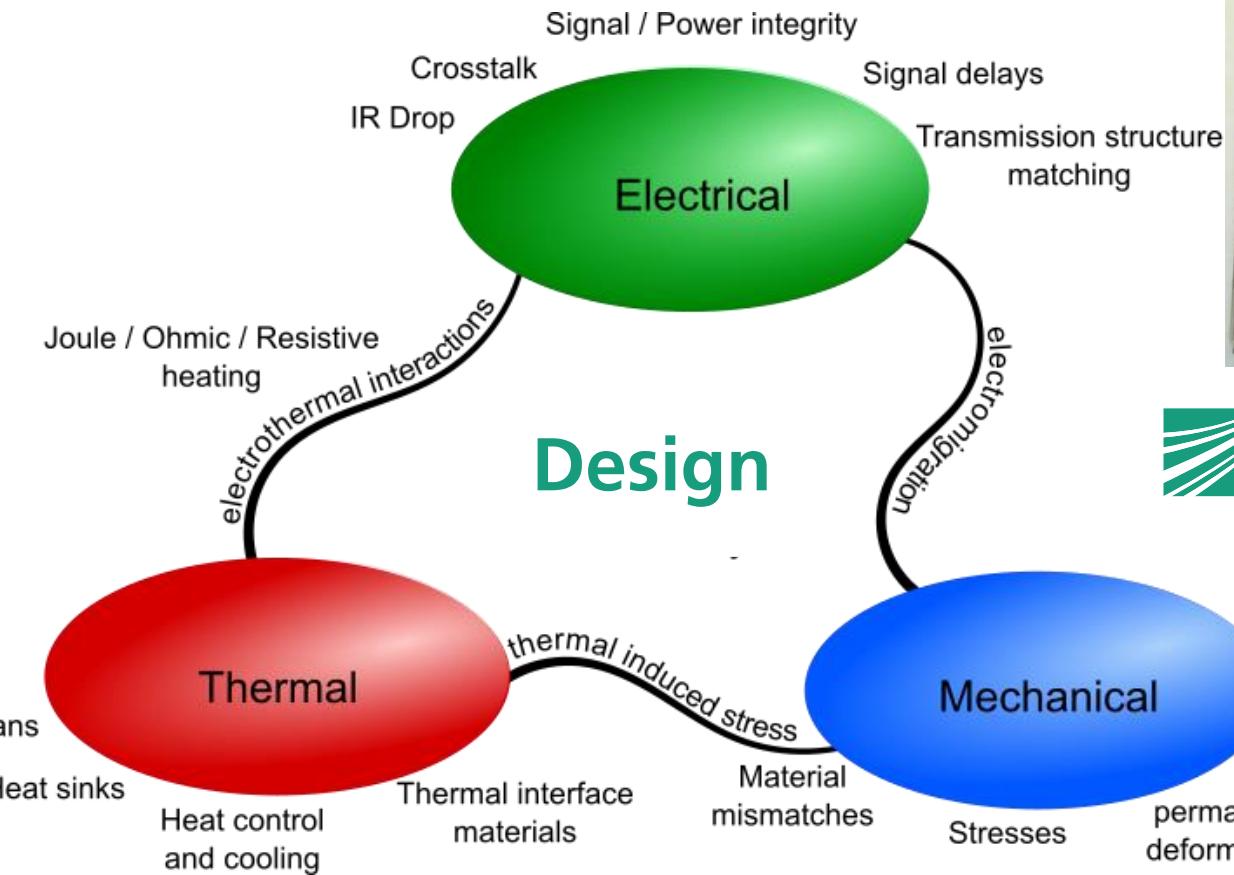
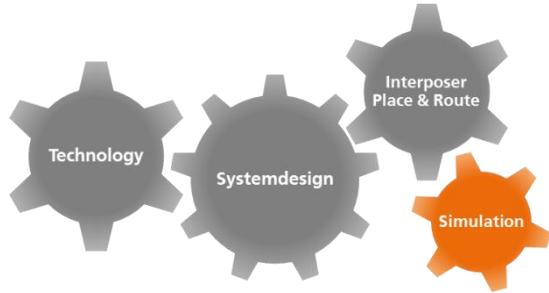
3D Integration – Impact on System



Source: A. Wilde, P. Schneider, P. Ramm, DTC 2010

Simulation-based Validation

Consideration of Multi-Physical Domains

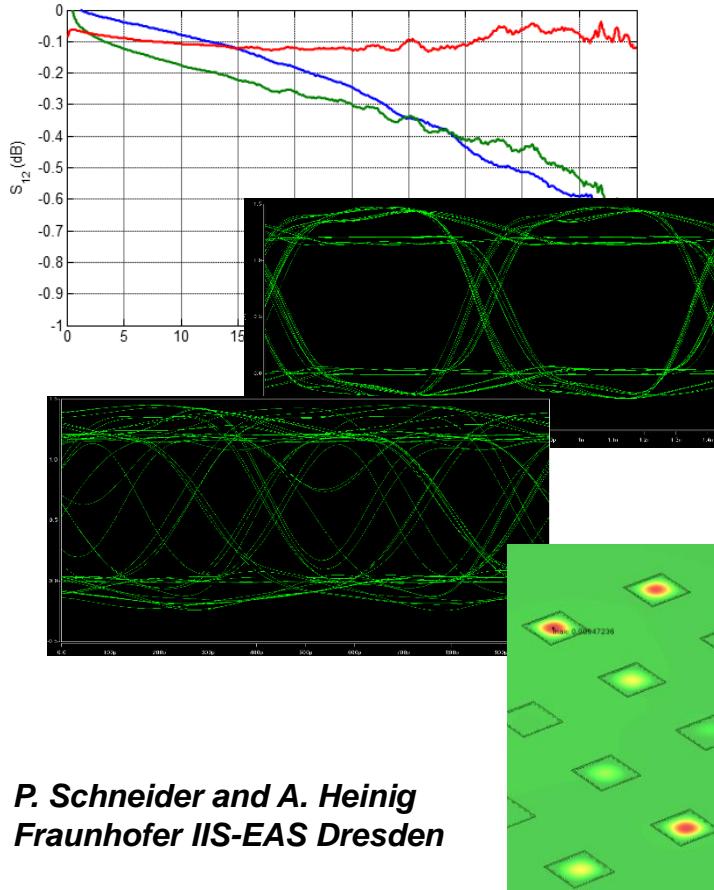
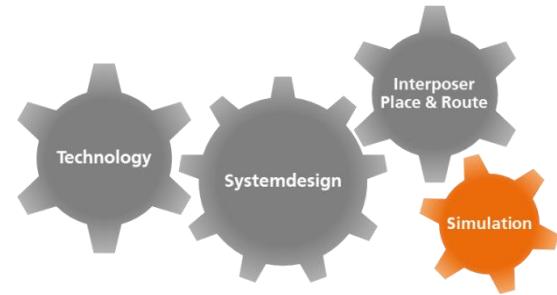


 **Fraunhofer**
IIS

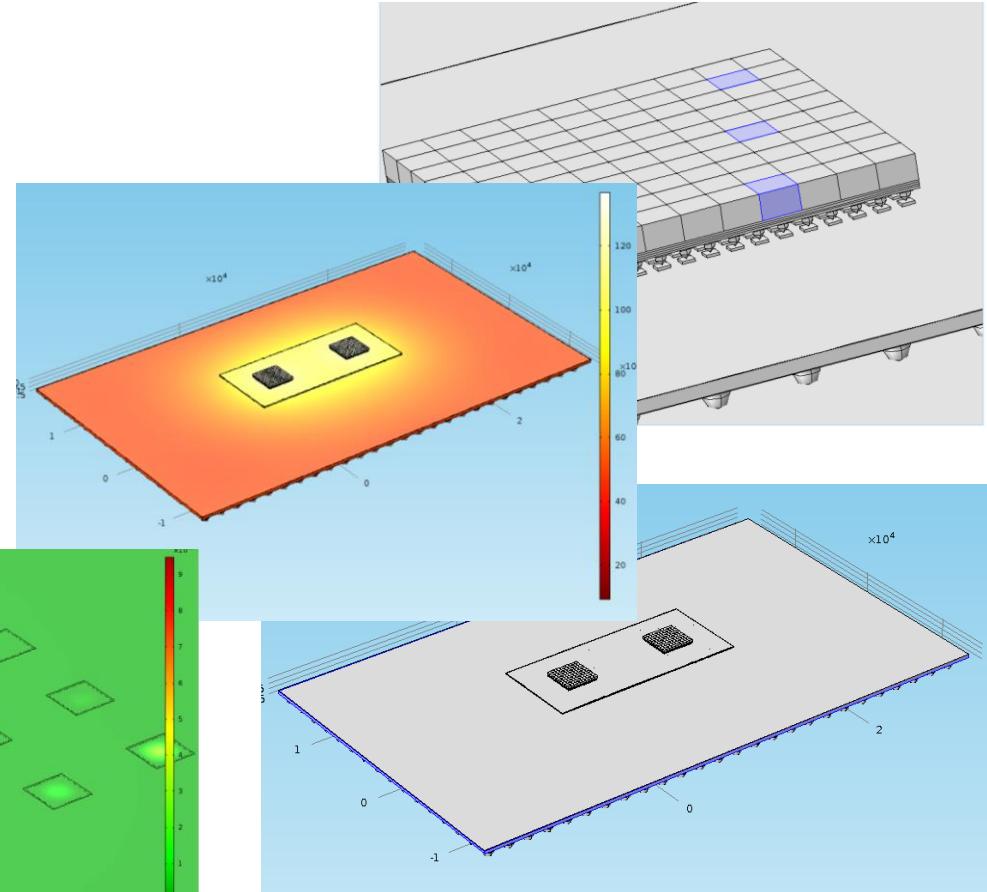
*P. Schneider and A. Heinig
Fraunhofer IIS-EAS Dresden*

Simulation-based Validation

Electrical, thermal and mechanical simulations



P. Schneider and A. Heinig
Fraunhofer IIS-EAS Dresden



3D Integration – Impact on heterogeneous systems

Physics of failure approach

Dedicated test vehicle to study degradation mechanisms

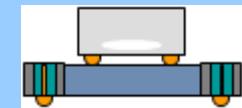
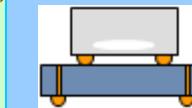
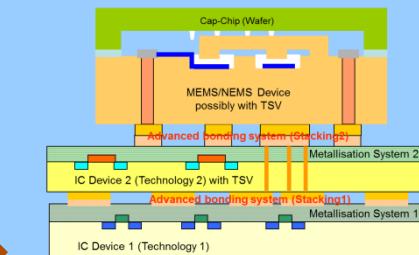
Built in reliability

- Material selection
- Low temperature bonding
- Protection against corrosion
- Robust processing
- No further stress tests



Innovative 3D applications

3D MEMS/NEMS & IC Integration



Quantification of stress by Micro-Raman Measurements at IMEC on W-filled TSV-SLID samples of Fraunhofer EMFT

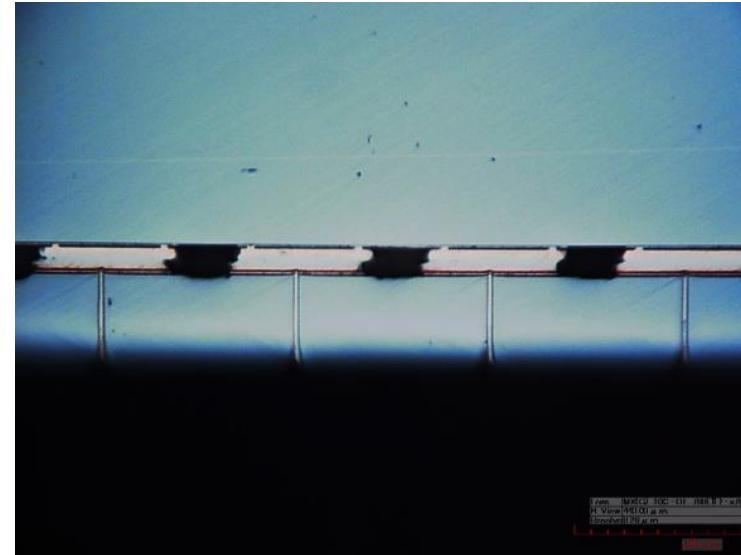
Micrograph of TSV-SLID test-samples of Fraunhofer EMFT:

Bottom-Silicon

SLID solder-bump (Cu-Sn-Cu)

W filled TSV within

Top-Silicon (thickness 50 μm)



How large is the stress imposed in Si due to this interconnect system?

Two stress sources were examined: W-filled TSV , Cu-Sn SLID solder bump

Quantification of stress by Micro-Raman Measurements at IMEC on W-filled TSV-SLID samples of Fraunhofer EMFT

σ_{radial}

Stress source: W-filled TSV

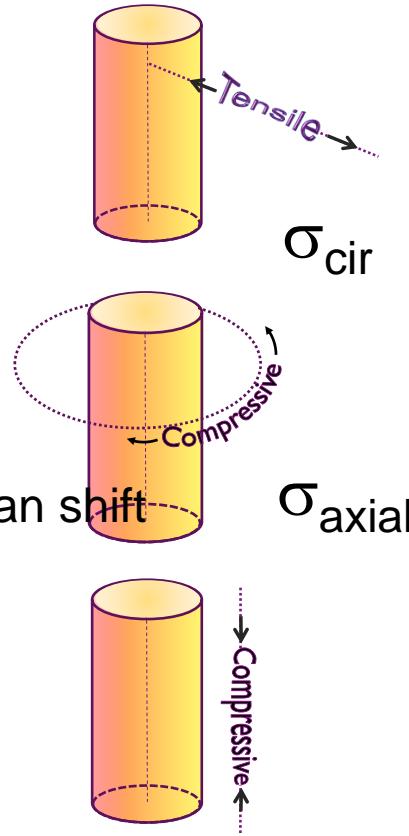
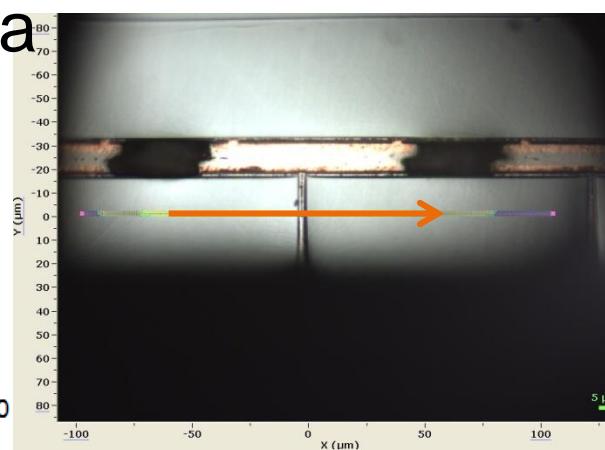
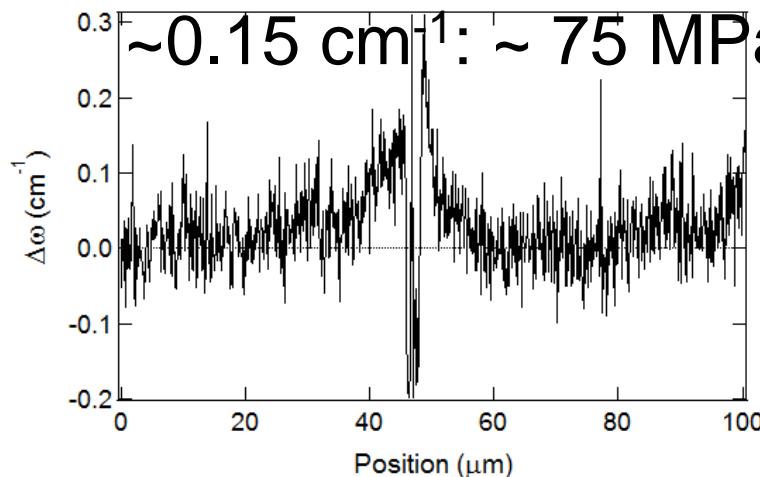
Assume W tensile: TSV wants to shrink

Expected to give in the nearby Si

- ▶ Tensile radial stress (σ_{radial})
- ▶ Compressive stress around the periphery (σ_{cir})
- ▶ Compressive stress along the length axis (σ_{axial})

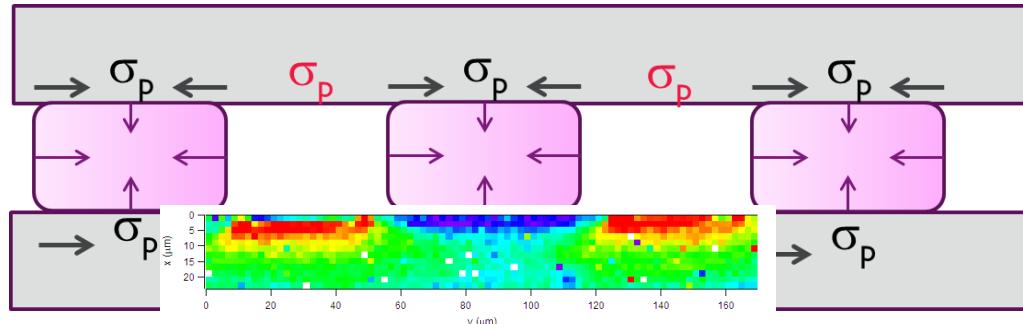
Because $\sigma_{\text{radial}} \approx -\sigma_{\text{cir}}$

Raman shift is dominated by σ_{axial} = compressive \rightarrow positive Raman shift



I. De Wolf, IMEC
J. Weber, Fraunhofer EMFT

Quantification of stress by Micro-Raman Measurements at IMEC on W-filled TSV-SLID samples of Fraunhofer EMFT



2D Raman measurement confirms compressive stress above SLID bump and tensile stress in between (~ 100 MPa)

Conclusion:

SLID-Bump

- Induces compressive stress in the Si under the solder and tensile in between the solder bumps.
- The magnitude of the stress is of the order of 100MPa but depends on dimensions and pitch of the SLID bumps

W-filled TSV

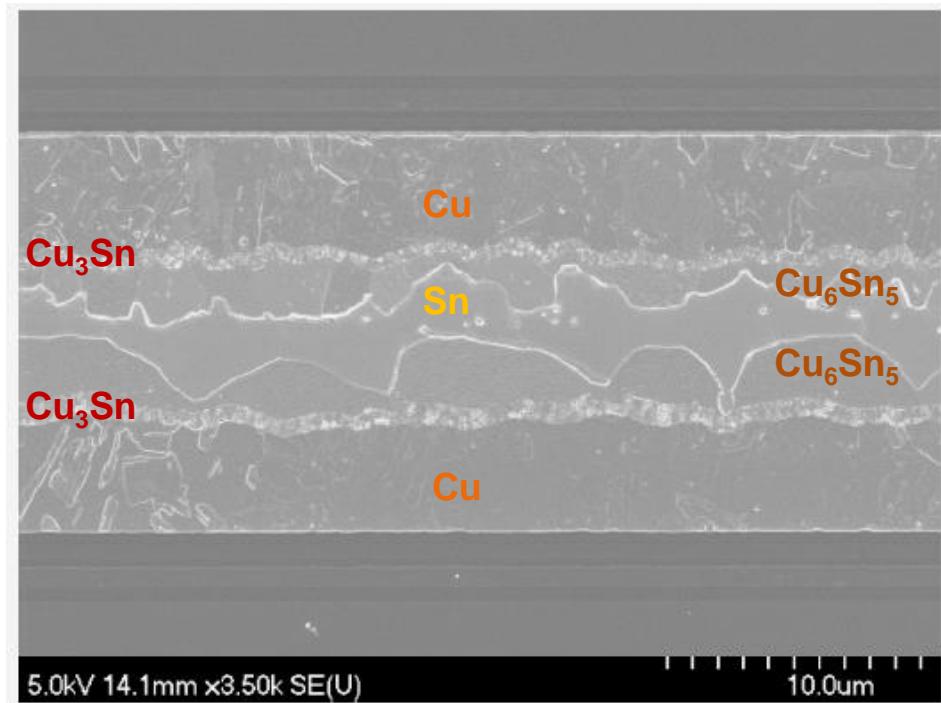
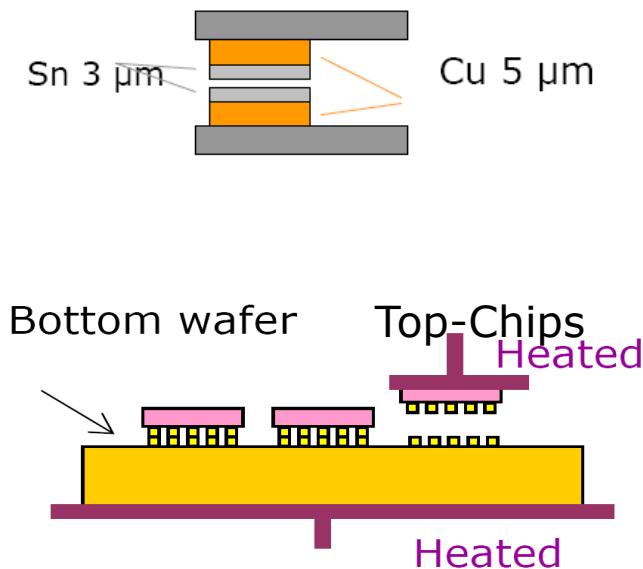
- Induces compressive stress along the axial direction and tensile stress along radial direction in the Si.
- The stress level seems small, order of 75 to 100MPa

I. De Wolf, IMEC
J. Weber, Fraunhofer EMFT

Novel Low-Temperature IMC Bonding Process (Cu/Sn)

Bonding at sub-melting temperatures with simultaneous ultra-sonic agitation (Panasonic Bonder FCB 3)

Cu/Sn IMC Bonding at 100 °C and 150 °C investigated.



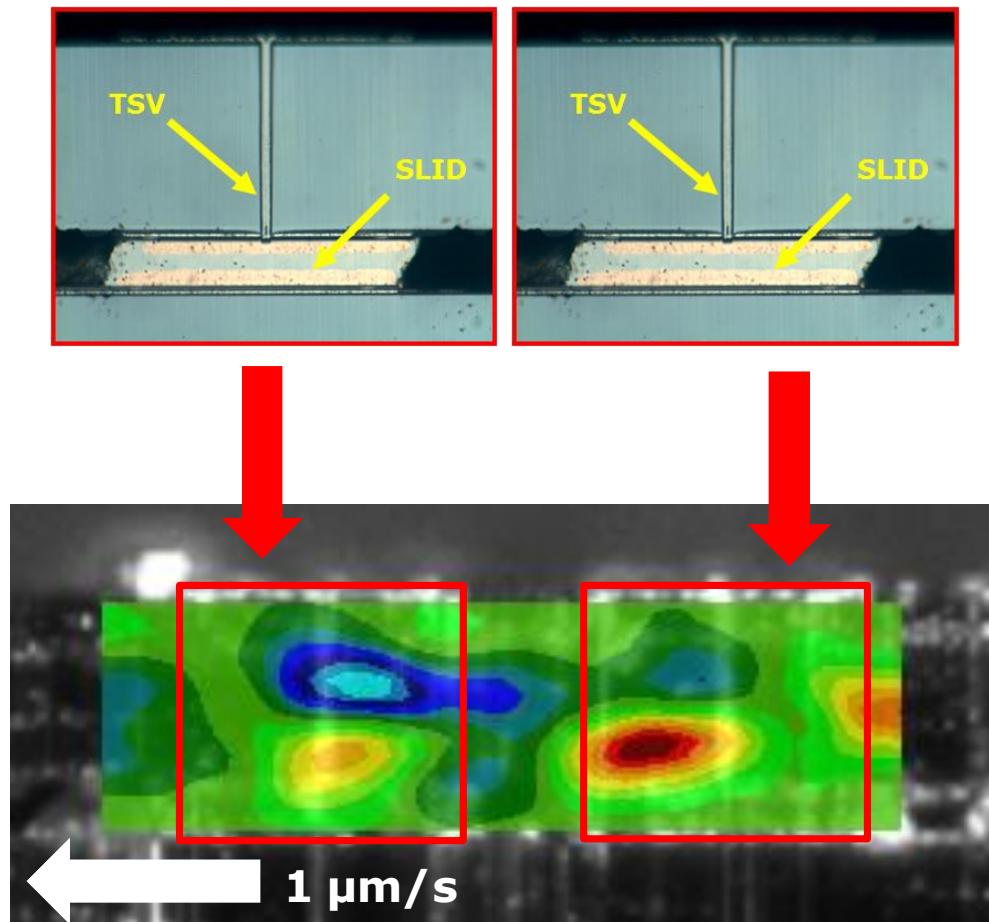
Ultrasonic supported Low temperature (150°C) Cu-Sn SLID Bond

Investigation of Low-Temperature IMC Bonding (Cu/Sn)

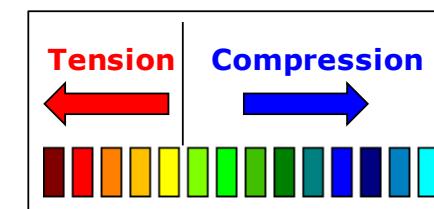
Panasonic FCB 3 Bonder: ultrasonic power 1.5 W, 50 s time, 20 N force
@ 150 °C bonding temperature:

- Shear forces of 17 MPa
- 50 % higher fracture toughness compared to reference (280 °C)
- Alignment accuracy: 3 μm

Quantification of deformation under shear load on W-TSV / Low-T SLID samples of Fraunhofer EMFT (Infineon)



Y-Strain after
Displacement of ~10
μm (10x)



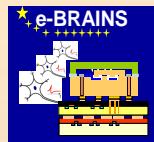
(uniDAC image)



3D History at Fraunhofer Munich

A Selection of Large Projects on 3D Integration (3)

2010 – 2014: European Large-Scale Integrating Project (ICT)



Infineon, Siemens, SORIN, 3D-PLUS, IMEC, CEA, Fraunhofer, ...

e-BRAINS – Best-Reliable Ambient Intelligent Nanosensor Systems by Heterogeneous Integration

→ Application Demonstrators for **3D Heterogeneous Systems**

→ Fine Pitch **3D-TSV Based HF Components** for RF MEMS

2014 – 2017: European NMP Project



Tyndall, SORIN, 3D-PLUS, KU Leuven, TUe, PSUD, Fraunhofer EMFT, ...

MANpower – Integration of Energy Harvesting and Storage for Perpetually Self-Powered Heterogeneous Systems (e.g. Leadless Pacemakers)

→ **Low-Temperature 3D Processes** for Highest Reliability Requirements

ECTC 2015: Fine Pitch 3D-TSV Based High Frequency Components for RF MEMS Applications

Summary & Conclusions

- We developed the technology for fine-pitch high-aspect ratio tungsten-filled TSVs in high-resistivity silicon substrates.
- The introduced TSV technology enables high performance RFIC applications, as demonstrated by the fabrication and characterization of wideband mm-wave antennas.
- The proposed technology is fully compatible with RF MEMS post-processing, allowing to envision 3D heterogeneous integration of high-performance, low power, compact tunable RF front ends.

Acknowledgements

This work was supported by the European Union's FP7 Large-Scale Integrated Project e-BRAINS ICT-257488



Dr. Peter Ramm, Fraunhofer EMFT Munich

IEEE 65th ECTC – San Diego, CA, USA

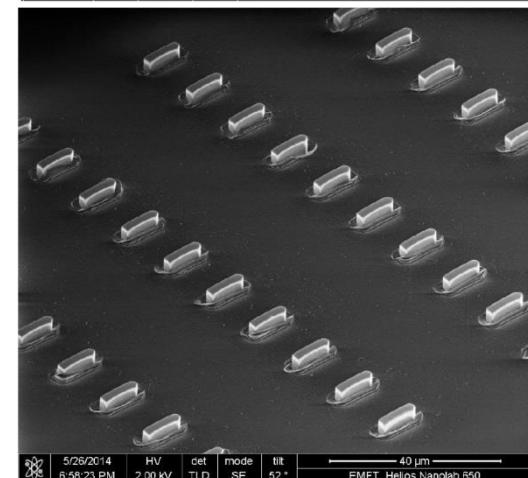
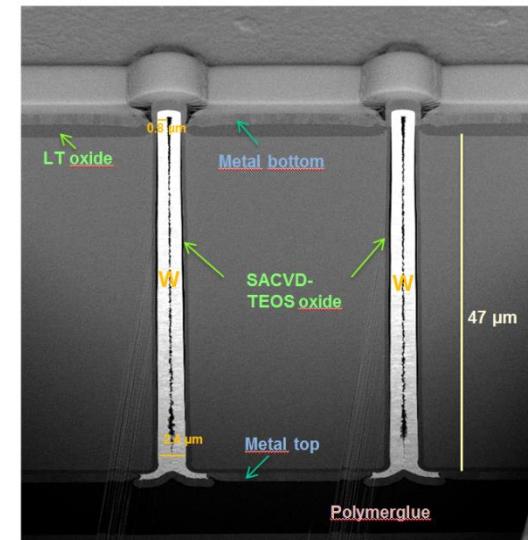
Wolfgang Vitale

May 26 – 29, 2015 27



Dr. Peter Ramm

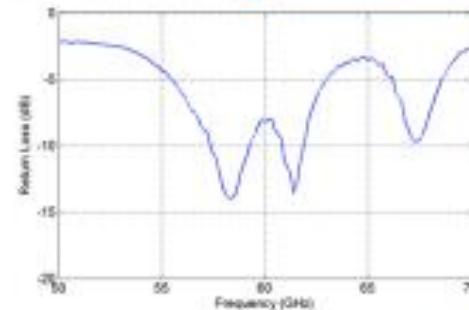
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ECTC 2015: Fine Pitch 3D-TSV Based High Frequency Components for RF MEMS Applications

Integration of mm-wave antennas: results

- RF characterization was performed up to 110 GHz using a VNA and LRRM calibration.
- The frequency response in the 50-70 GHz band matches the expected results.
- The surface-wave and radiation loss in the front-to-back transition amounts to 1.5 dB.



Dr. Peter Ramm, Fraunhofer EMFT, Munich

IEEE 66th ECTC – San Diego, CA, USA

Wolfgang Vitale



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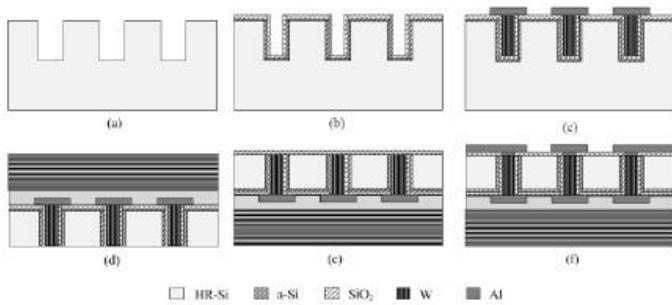


Fig. 1 Main steps of the fabrication process flow. (a-c): top-side processing; (d-f): bottom side processing.

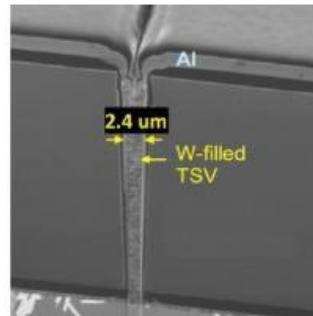


Fig. 2 cross-section of a W-filled TSV

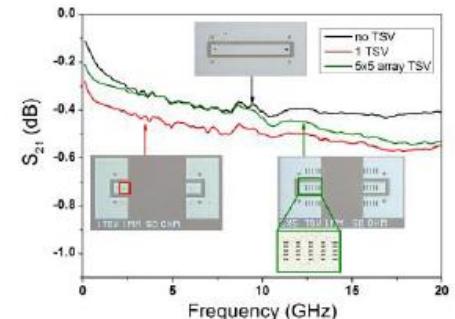


Fig. 3. Effect of two TSV transitions on S-parameters for 1 mm long CPWs.

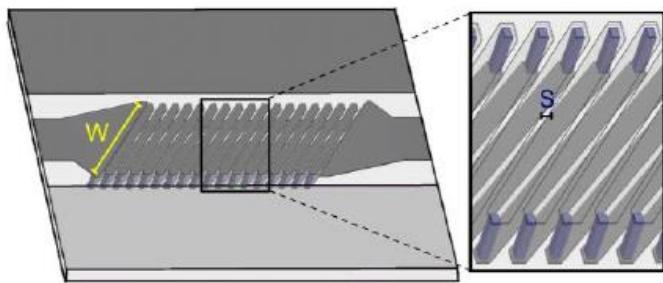


Fig. 4 Inductor schematic diagram with zoom on TSV coil structure, highlighting the coil width *W* and spacing between signal lines *S*.

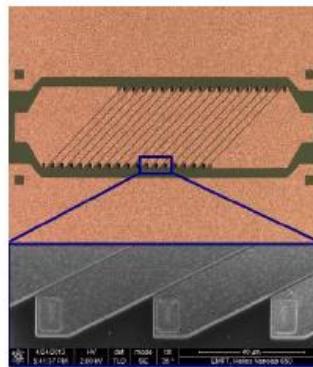


Fig. 5: Top view of a fabricated integrated inductor, with zoom on TSVs at the end of signal lines.

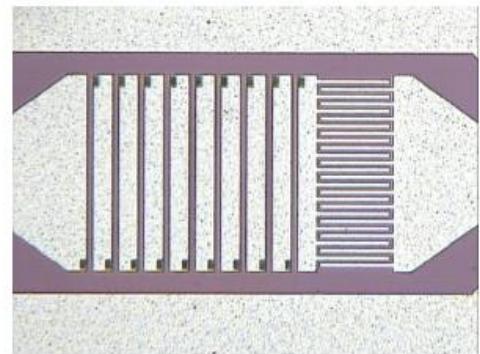
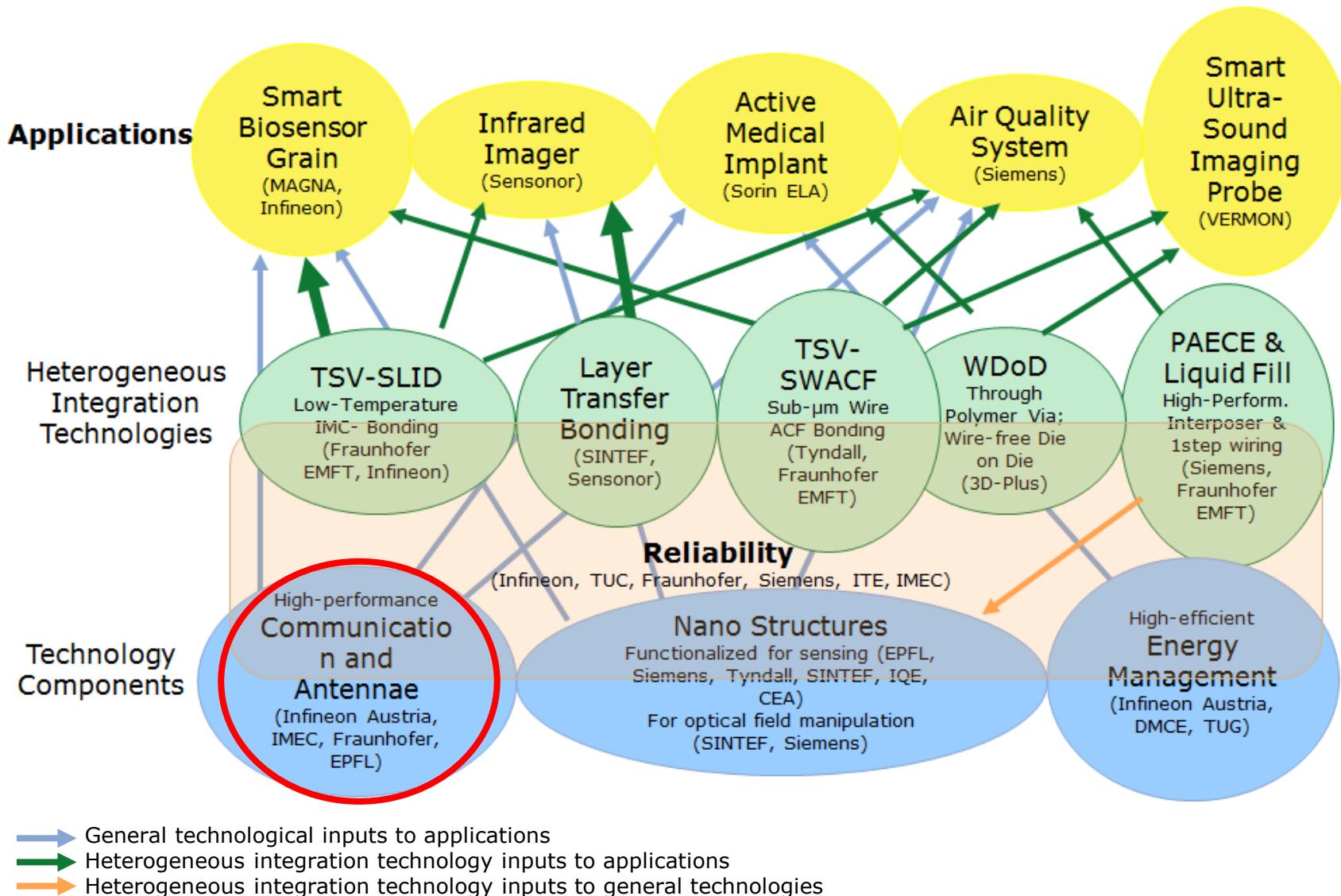
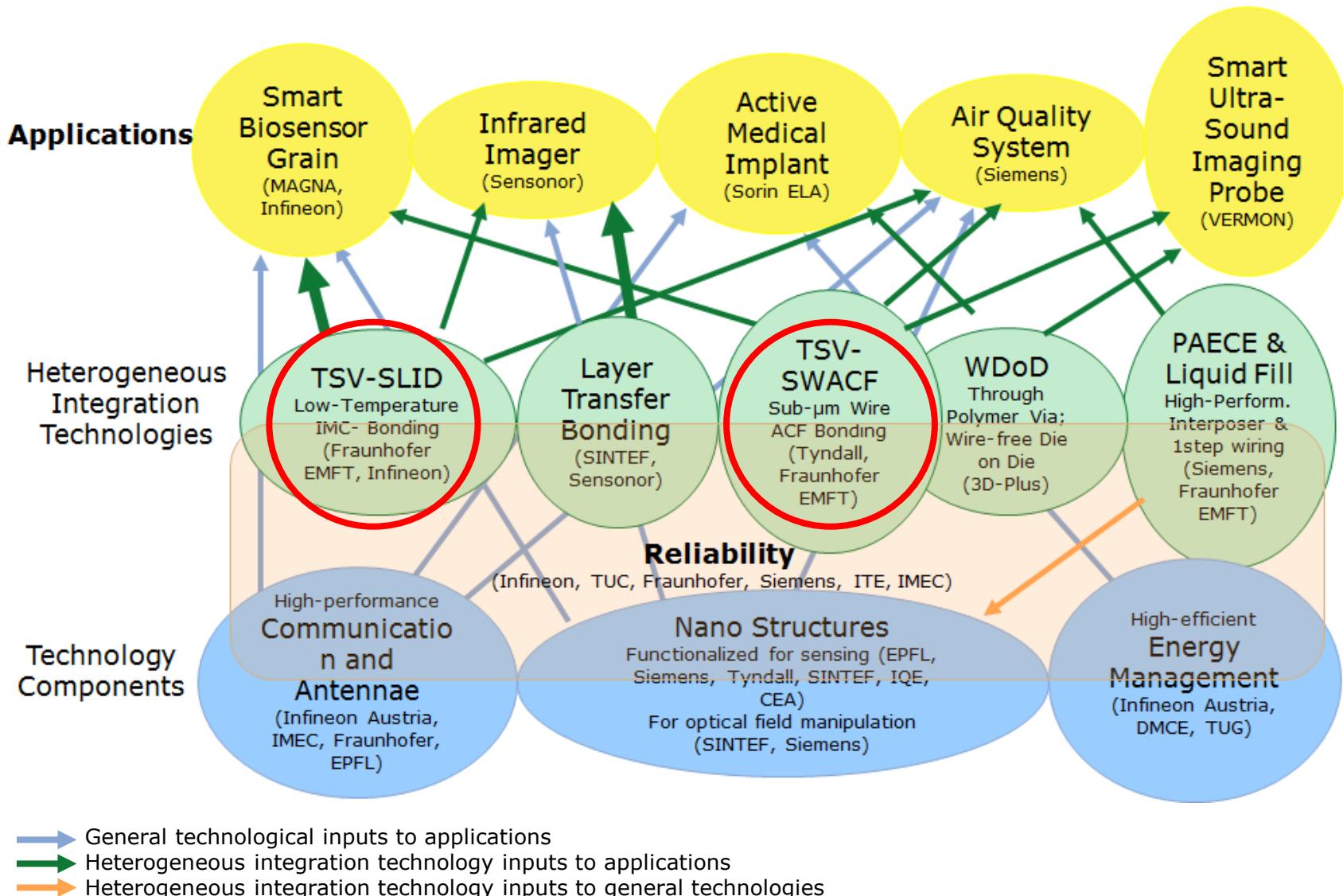


Fig. 6: Top view of an LC resonator employing a TSV inductor and an interdigitated capacitor.

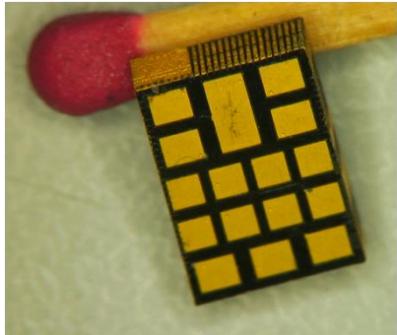
Technology Platform and Applications in e-BRAINS



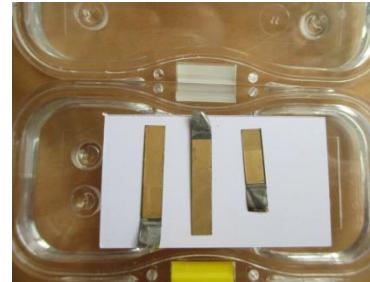
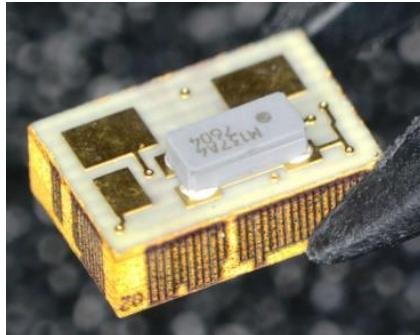
Technology Platform and Applications in e-BRAINS



App3: Active Medical Implant (Leadless Ultra-Miniaturized Pacemaker)



3D IC heterogeneous integration



Piezo-Harvester (20x6mm)



Finally assembled Pacemaker module

- Successful in-vivo evaluation (battery driven module)
- Piezo-Harvester: First successful in-vivo demonstration



Clinical trials

Our Future Work in 3D IC:

3D TSV Technologies for RF-MEMS & RF-ICs and for Heterogeneous Integration (e.g. Medical Applications)

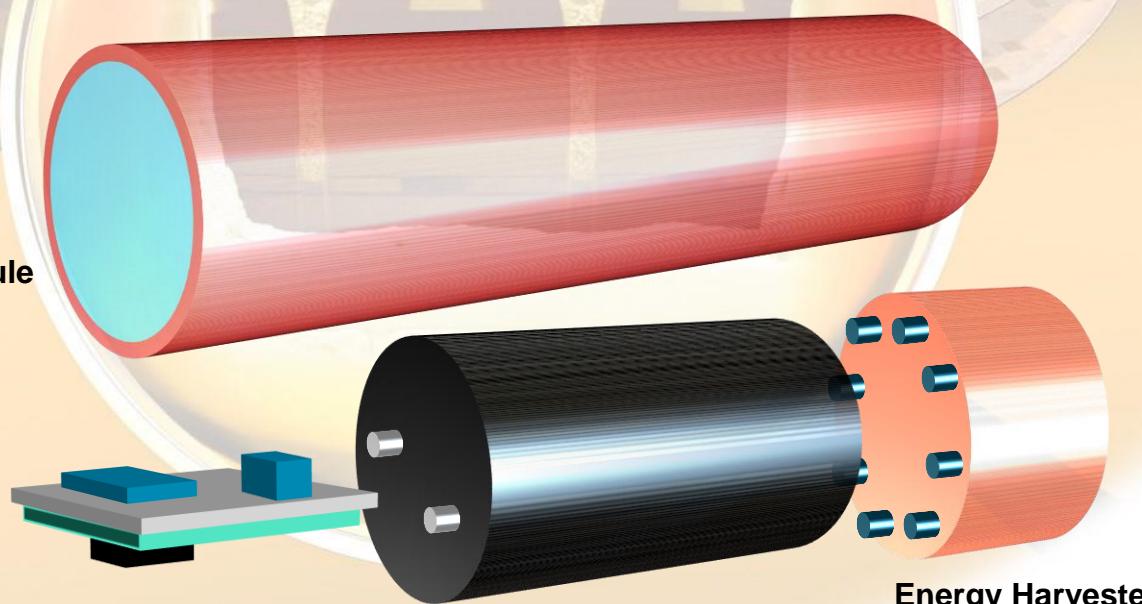


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MANpower – Integration of Energy Harvesting and Storage for Perpetually Self-Powered Heterogeneous Systems (e.g. Leadless Pacemakers)

→ **Low-Temperature 3D Processes** for Highest Reliability Requirements

Leadless Pacemaker Capsule



3D Integrated IC/Sensor System

Supercap

Energy Harvester

Summary

- Our early work at Fraunhofer Munich and Siemens/Infineon on
 - 3D CMOS Devices
 - Performance and thermal issues of 3D-ICs
 - TSV processes
 - Wafer thinning & thin die handling
 - Wafer bonding
 - Die-to-wafer stacking technologies (KGD)
- 3D integration technology is now entering a mainstream
 - Memory stacks, memory/logic, ... (high density TSVs)
 - Heterogeneous sensor/IC integration (medium density TSVs)
- Choice of 3D process depends on
 - Performance, TSV/pad pitch requirements
 - Reliability requirements
- Our ongoing work is focussed on TSV based RF-MEMS & RF-IC and **Highly reliable** ultra-low power **3D heterogeneous MEMS/IC** systems

Thank You For Your Attention !



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