

3D Architectures for Semiconductor Integration and Packaging (3D ASIP), Burlingame, CA, Dec. 10-12, 2014



*Preconference symposium-
3D Integration: 3D Process Technology*

TSV Formation: Drilling and Filling

Dean Malta, Alan Huffman*
RTI International
Research Triangle Park, NC
dmalta@rti.org

(*presenting author)

Dec. 10, 2014



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3D ASIP December 10-12, 2014, Burlingame, California

Introduction

Basic TSV Requirements

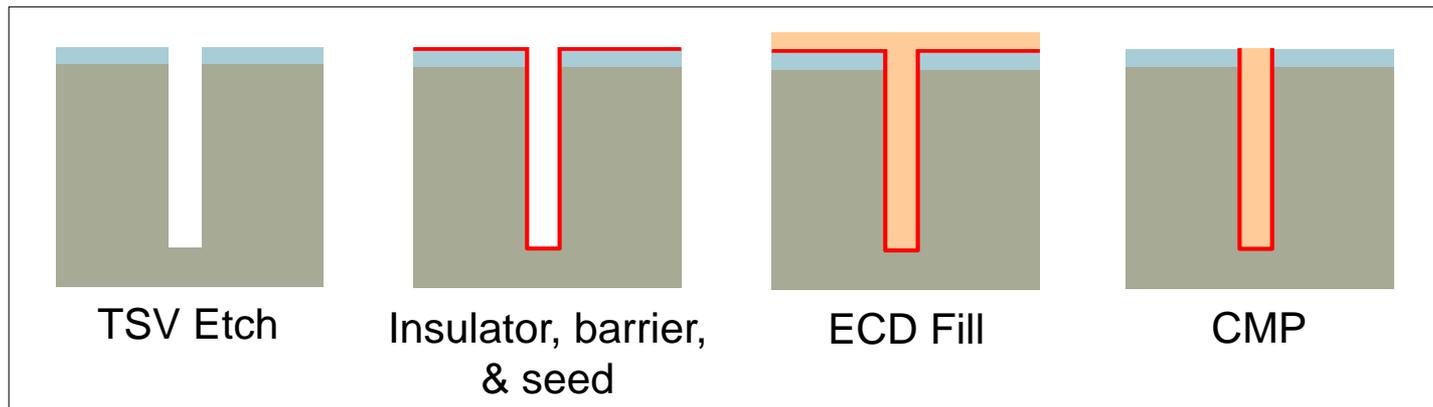
- Low resistance & capacitance
- High reliability
- No impact on device operation
- High process throughput & yield
- Low added cost

While TSV technology has greatly matured, cost remains a significant challenge for widespread implementation

TSV “Drilling & Filling” Steps

Basic process flow for Cu TSV drill & fill:

- High aspect ratio TSV etch (DRIE)
- Conformal oxide insulator deposition (typ. CVD)
- Barrier and seed layer deposition (typ. PVD)
- Copper via fill (ECD)
- Overburden removal (CMP)



Typical via-middle TSV process

TSV Implementation Examples

- **CMOS image sensor** – first volume TSV implementation
- **Si interposer** (2.5D integration)
- **3D applications**
 - 3D memory stacks
 - Memory-logic
 - Wireless modules
- **MEMS wafer level package, optics, other...**

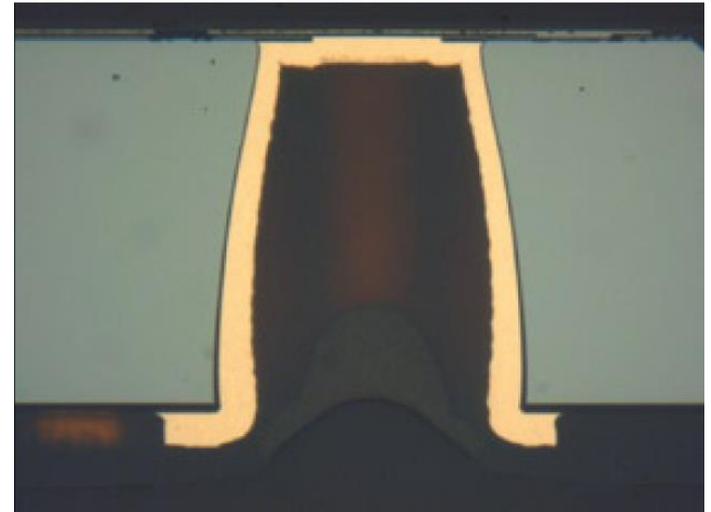
Some differences in TSV implementation by application

TSV for CMOS Image Sensor (CIS)

Early TSV in CIS: beginning ~2008

CMOS image sensor is a unique case for TSV:

- Relatively large, low aspect ratio TSVs (~2:1)
- Backside TSV-last process
- Often tapered TSV profile (easier deposition of liners)
- Often uses unfilled TSVs (metal lined)



Backside TSV in CMOS image sensor (Toshiba)

TSV drill and fill processes for CIS are different than higher density TSV applications (such as interposer and 3DIC)

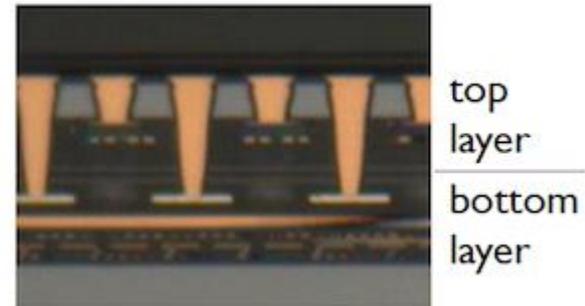
TSV for CMOS Image Sensor (CIS)

Recent evolution of TSV in CIS:

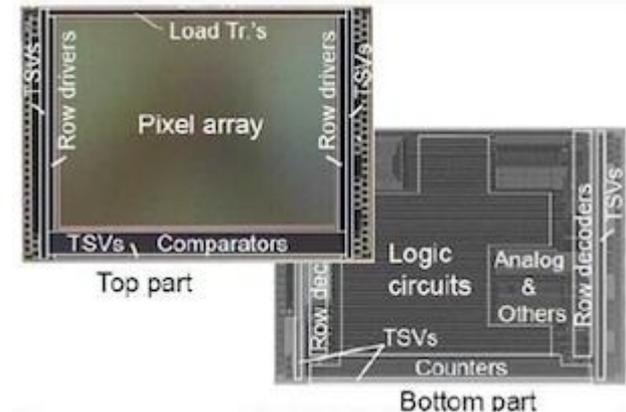
Stacked backside illuminated CMOS image sensor (Sony):

- Dual TSV connections (to pixel and logic layers)
- Smaller TSVs (6 um pitch)
- Filled via process
- Slightly higher A.R. (logic TSV connections)
- Still backside process with tapered TSV profile

Cross section (from Chipworks)



Circuit Layers:

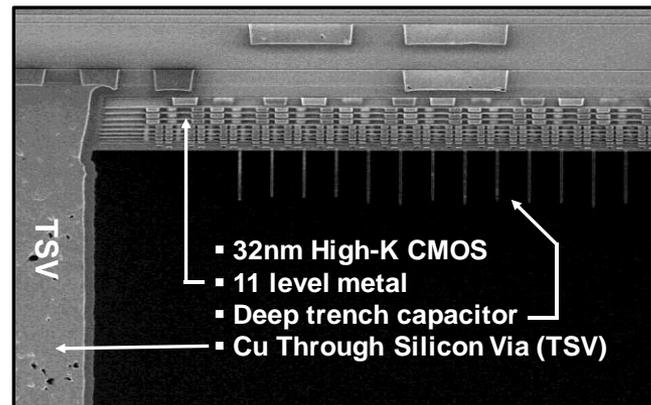
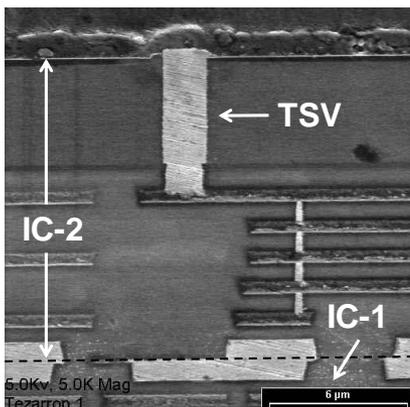
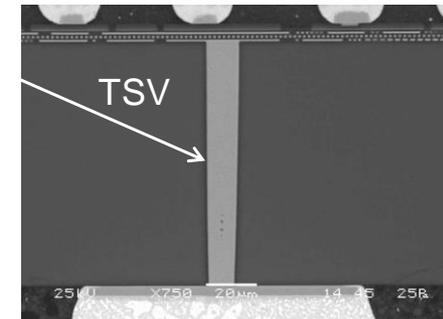
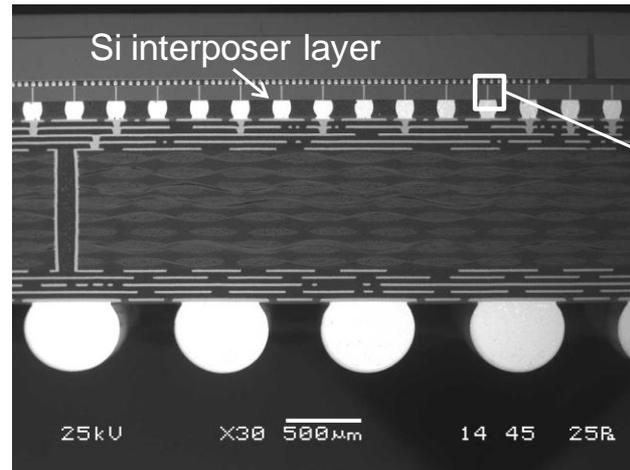


Stacked backside illuminated CIS with TSVs (Sony)

TSV for Interposers and 3DIC

TSV in Si Interposer:

Xilinx / TSMC / Amkor
2.5D Wide I/O FPGA on Si
interposer, attached to organic
substrate



TSV in 3D IC:

Left- Tezzaron 3D processor
with tungsten TSVs

Right- IBM embedded DRAM
with Cu TSVs

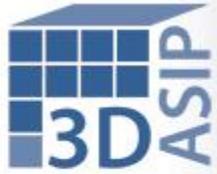
TSV for Interposers and 3DIC

Implementation differences for Si interposer Vs. 3DIC:

- Typically larger TSV dimensions for interposer
- No transistor keep out zones (KOZ) or thermal process limitations for passive interposers

	3DIC	Si Interposer
TSV dimensions:	Typ. $\leq 5 \times 50$ μm	Typ. $\leq 10 \times 100$ μm
Process Thermal Budget:	$\leq 400^\circ\text{C}$ due to transistors	No process temp limit. Higher temp liners (E.g., thermal oxide) may be used.
Design Considerations:	Possible transistor effects- requires KOZ	No KOZ (assuming no actives on wafer).

Etch, fill, and reveal steps tend to be similar-- liners may differ.



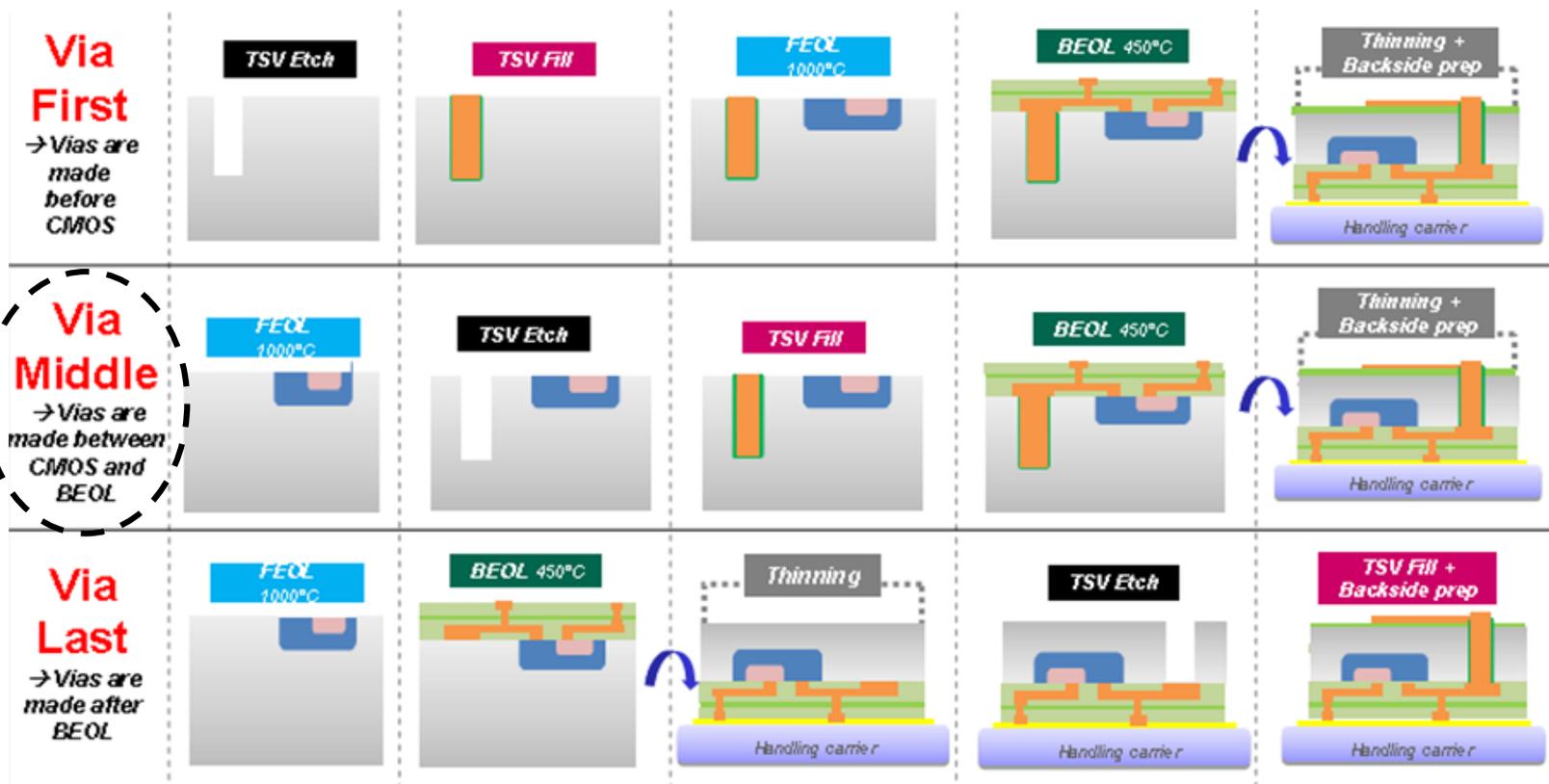
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TSV Integration Approaches for 3D

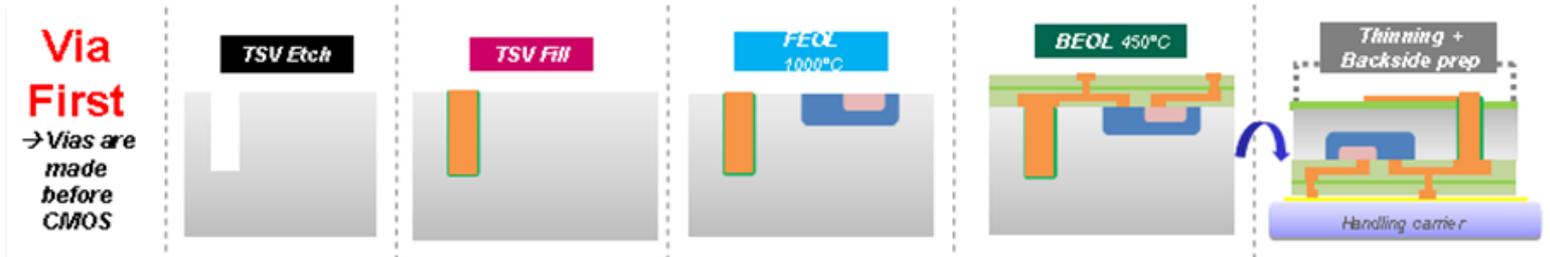
Overview of Approaches

- Historically, 3 options have been considered for TSV implementation in IC wafers:



(image courtesy of Yole Développement)

Via First



- TSVs fabricated before active devices (FEOL)
- TSV materials must be compatible with subsequent transistor fabrication process (at high temperature)
- Limits conductor choices- primarily poly Si
- Simple implementation- allows thermal oxide liner and no barrier required
- Via conductivity is a significant limitation

This approach has largely fallen out of consideration due to TSV conductor limitations

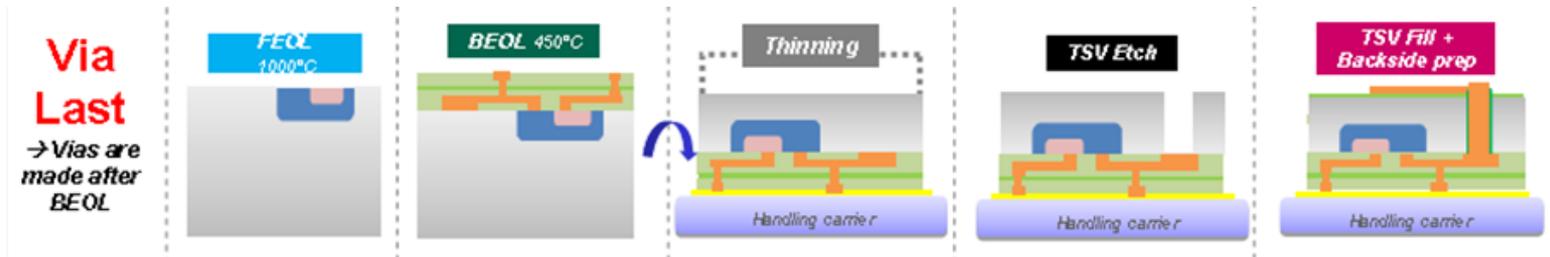
Via Middle



- TSVs fabricated after FEOL, before BEOL
- Limited process thermal budget (device compatibility, <math><400^{\circ}\text{C}</math>)
- Process challenges (largely addressed in recent years):
 - Low temp conformal dielectric, barrier, seed layers. High AR via fill.
 - Mechanical reliability (mainly Cu-Si CTE mismatch)
- Best overall combination of TSV properties and integration
- Cost remains a significant barrier

Via middle has largely emerged as the preferred high volume manufacturing (HVM) option for TSV

Via Last- Backside

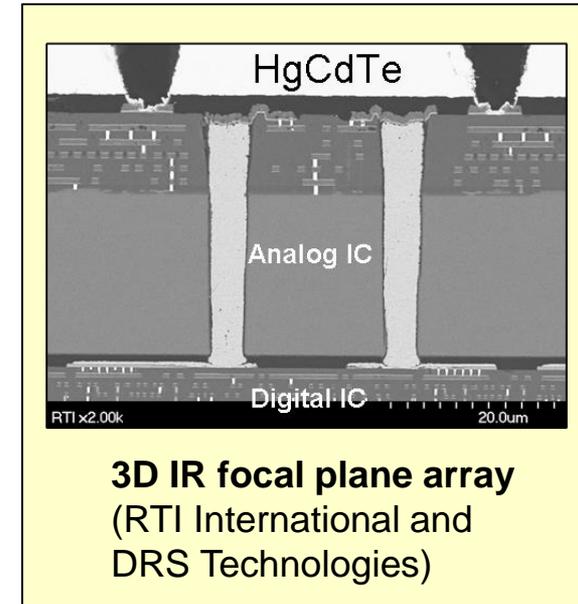


- Primarily used for CMOS image sensor (or other low AR applns)
 - AR typ. 2:1 to 3:1, often unfilled vias
- Low thermal budget (compatibility with temporary carrier, <200°C)
- TSV lands on frontside metal layer
- Limitations / challenges for high AR vias
 - Requires dielectric “bottom-clear” etch
 - Challenge making low resistance contact in high AR vias
 - Metal land surface affected by plasma, challenging to restore in high AR vias

Backside via last is used in selected applications (e.g., image sensor), better for low AR vias

Via Last- Frontside

- May apply to custom / niche applications requiring 3D performance (with high AR TSV)
- Enables 3D for wafer technologies not available with foundry via-middle TSVs
- TSVs may be etched from front (post IC foundry), then processed like via-middle
- Higher process cost and complexity
 - Design die with exclusion areas for later TSV integration
 - TSV etch goes through all BEOL dielectric layers
 - May require planarization of top IC metal (for TSV pattern & etch, Cu CMP)



Possible option for custom 3D applications, if less cost sensitive and TSV middle wafers are not available



3D Architectures for Semiconductor Integration and Packaging

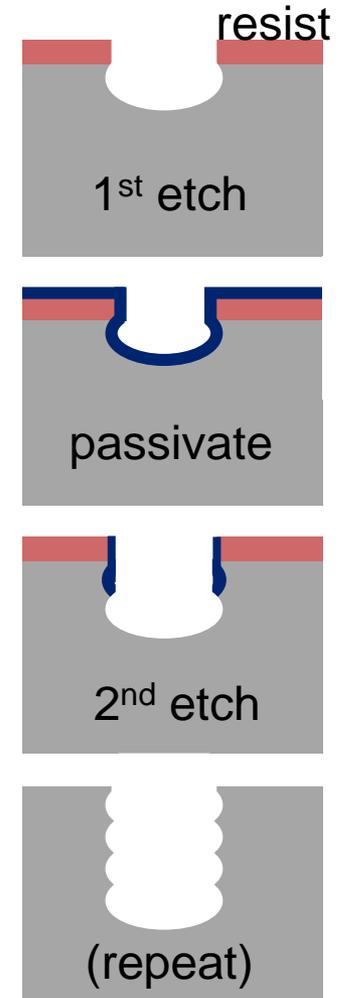
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TSV Fabrication Processes

TSV Etch- Process Methods

- Deep reactive ion etching (DRIE)
- Commonly uses Bosch™ process- alternating passivation and etch cycles
 - Short isotropic etch steps (typ. SF_6)
 - Passivation of sidewalls (C_4F_8 or similar)

- Key requirements:
 - High aspect ratio
 - High etch rate & uniformity
 - Low sidewall roughness (minimal scallops)
 - Precise control of sidewall angle ($\sim 90^\circ$)
 - Process cost



“Bosch” Process

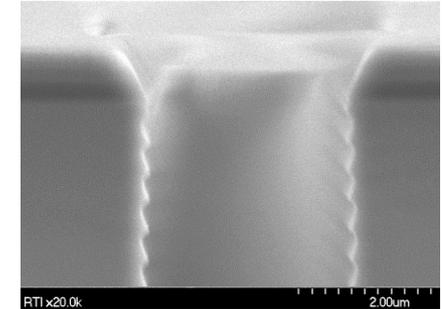
TSV Etch Advancements

Improvements in Equipment and Methods

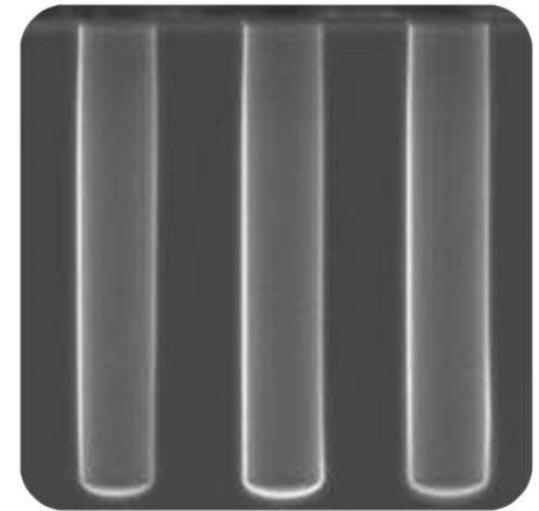
- Advanced plasma sources, MFCs, controls, pumping
- Fast switching enables short, stable etch & passivation cycles
- Process chemistry optimization

Resulting DRIE Improvements

- Higher etch rates
- Higher aspect ratio
- Precise profile control (sidewall angle)
- Smooth sidewalls- minimal or no scallops



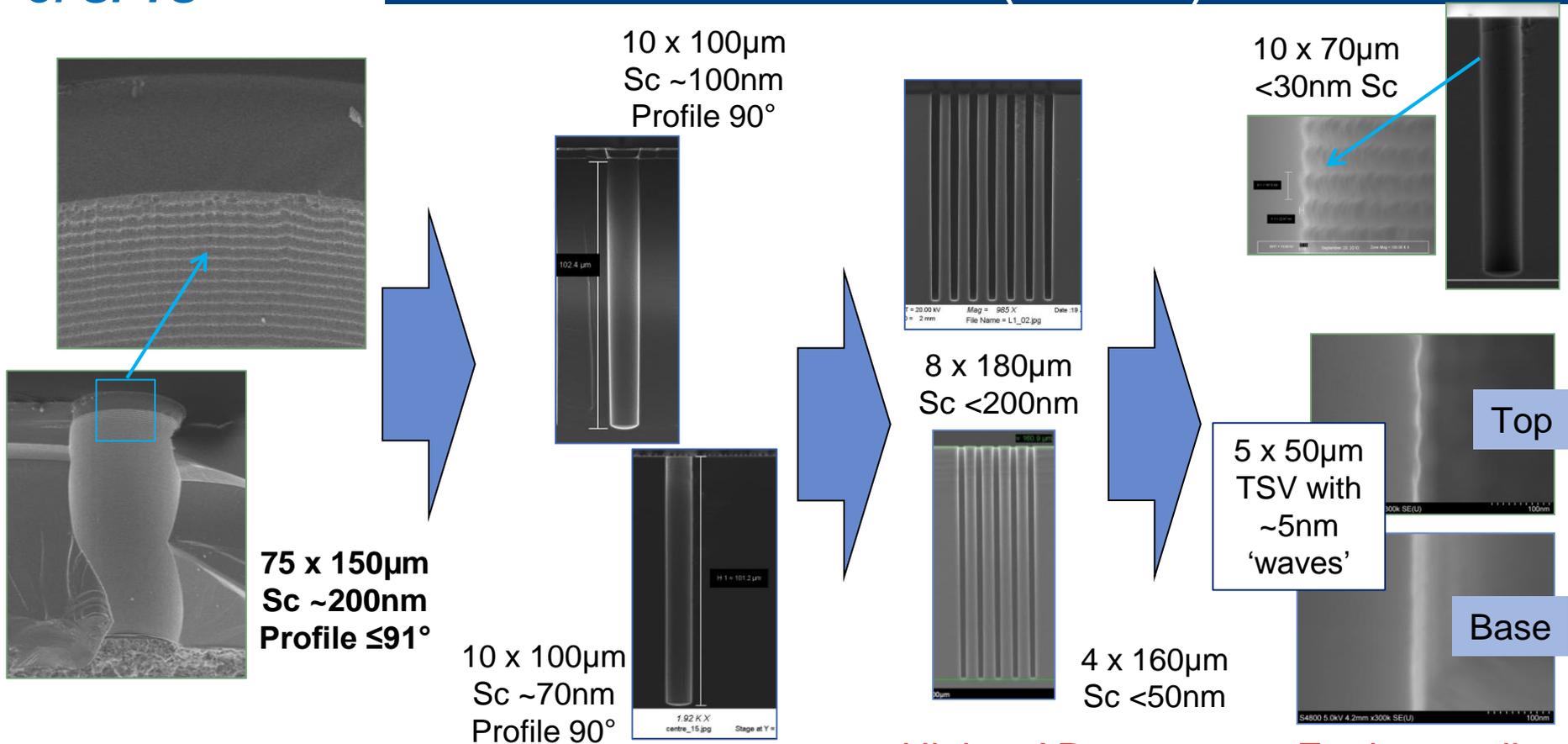
DRIE scallops (typical)



“Scallop-free” TSV etch (SPTS)

Data courtesy of SPTS

TSV Etch Evolution (SPTS)



Early capabilities:
Sc ~200-500nm
Profile <91-92°

Improved profile & scallops

Sc ~50-200nm
Profile 90°
AR: 10:1 - 40:1

Higher AR

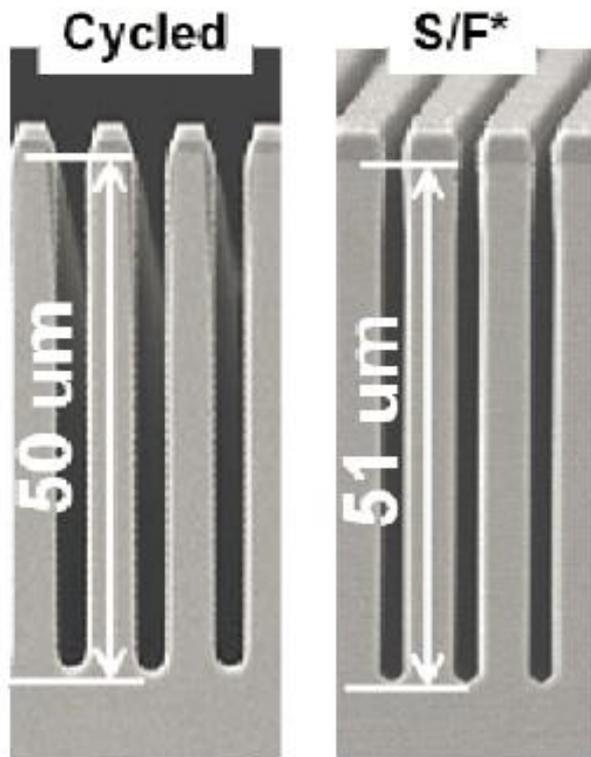
Further scallop reduction

Sc as low as 5 nm

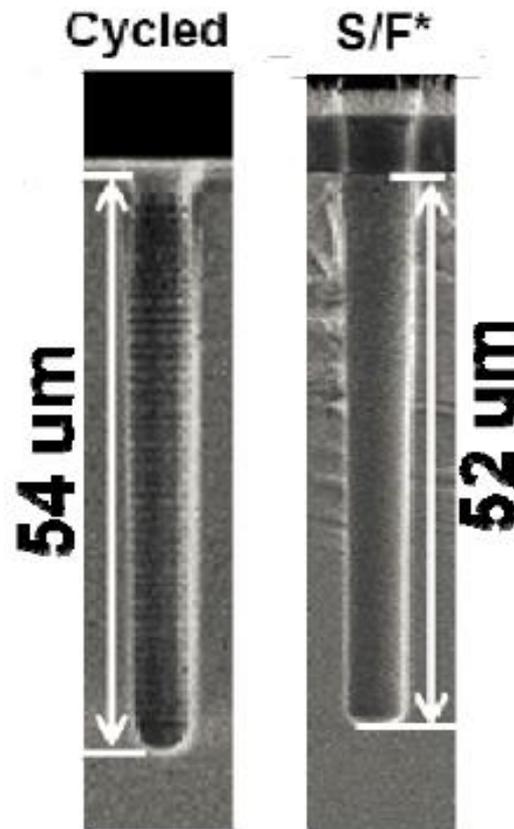
Alternative / emerging TSV etch methods

Scallop-free etch process reported by ULVAC:

a) 2 μm Space



b) 5 μm Hole



*S/F: Scallop-free

ULVAC's Scallop free process:
(2014 3DIC conference)

- Non-Bosch alternative
- Continuous etch (no separate passivation cycles)
- No FC chemistry. Uses SF_6 and O_2 .
- Sidewall passivated during etch by SiO_x
- Low sidewall roughness and impurities

TSV Insulator

- CVD oxide liner is typically used for via-middle 3DIC*
 - Often O₃/TEOS SACVD oxide (highly conformal), plus PECVD TEOS (for moisture resistance)

- Key requirements:
 - High deposition rate
 - Conformal deposition
 - Low dep temperature ($\leq 400^{\circ}\text{C}$)
 - Low stress
 - High breakdown voltage

(* for interposers, oxide can be thermal or CVD)

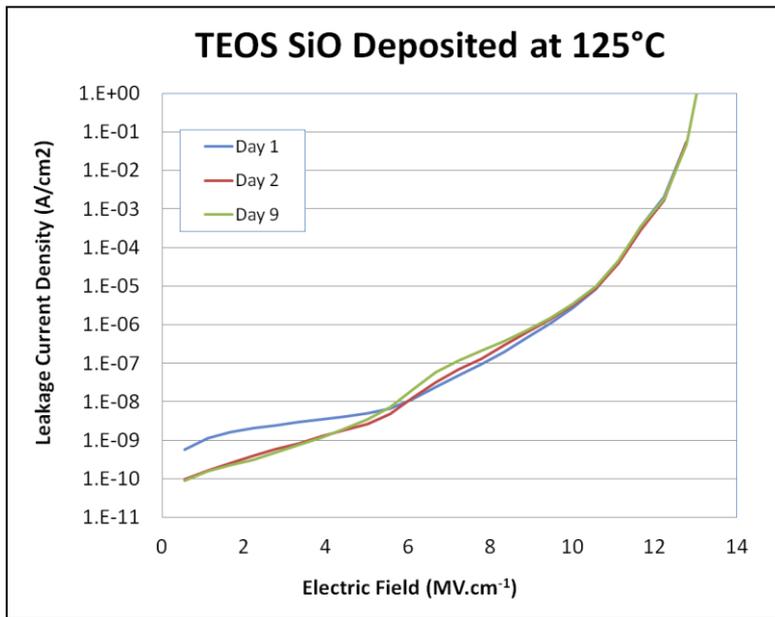


Conformal oxide in 10x100 um TSV (Applied Materials)

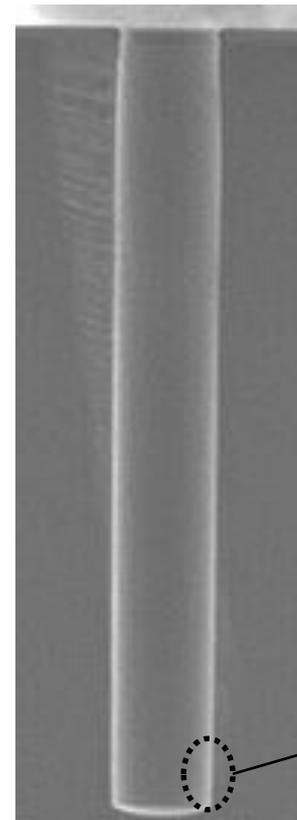
Data courtesy
of SPTS

TSV Insulator

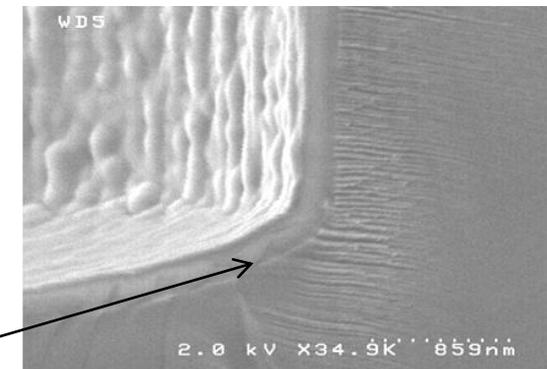
- SPTS developed a low temperature PECVD process suitable for backside TSV-last, using silane (for $AR \leq 2:1$) or TEOS ($AR > 2:1$)
- Deposition as low as 100°C , compatible with temporary carrier processing



Stable Leakage Current

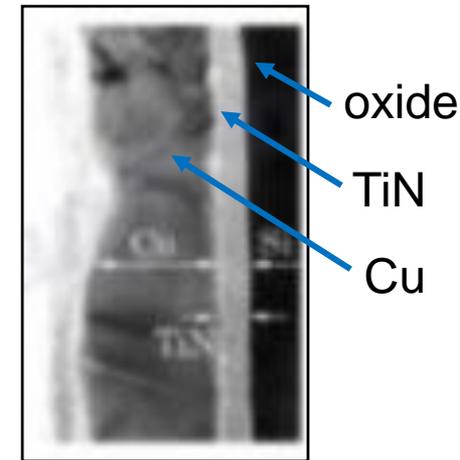


LT TEOS SiO
in $10 \times 80 \mu\text{m}$
TSV (SPTS)

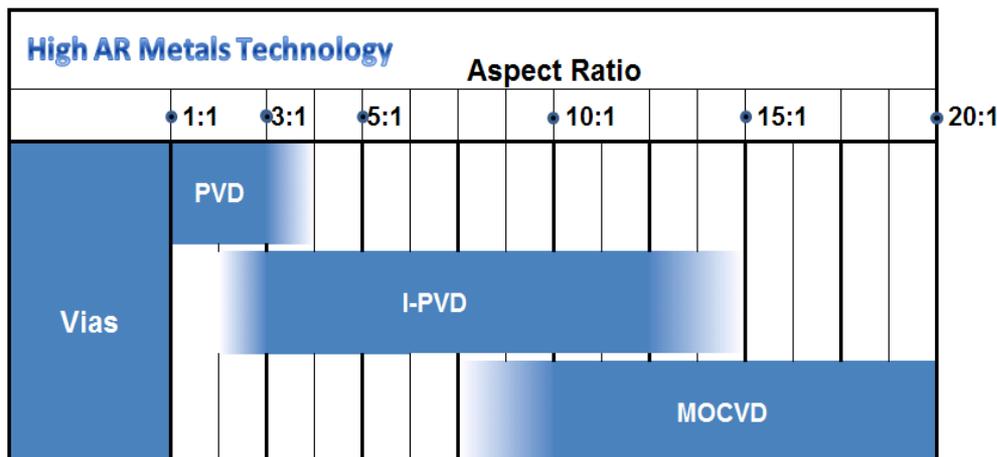


TSV Barrier / Seed

- Typically PVD used for barrier / seed
 - Standard PVD may be sufficient for low AR (approx. <math><3:1</math>)
 - Ionized PVD for higher AR (>3:1)
- Barrier-
 - Common choices may include Ti, TiN, Ta, TaN
 - Also provides adhesion layer for Cu via metal
- Copper seed layer
 - Should be conformal, minimize ECD potential drop



TiN barrier, Cu seed (ASET)



CVD and ALD barrier & seed options are emerging for higher AR vias (see future trends section)

TSV Filling

- Copper filling by advanced electrochemical deposition (ECD)
- Processes & equipment are specially developed for TSV

- Key requirements:
 - High deposition rate
 - Bottom-up, void-free fill
 - Low overburden thickness
 - Low impurities (e.g., C, Cl, O, S)
 - Low extrusion during anneal

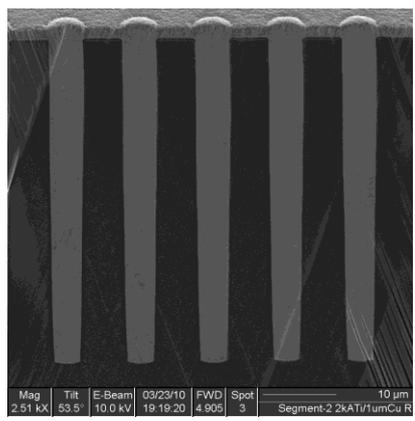
TSV ECD bath components:

1. Make-up solution with high Cu concentration
2. Organic additives may include:
 - a. Suppressor
 - b. Accelerator
 - c. Leveler

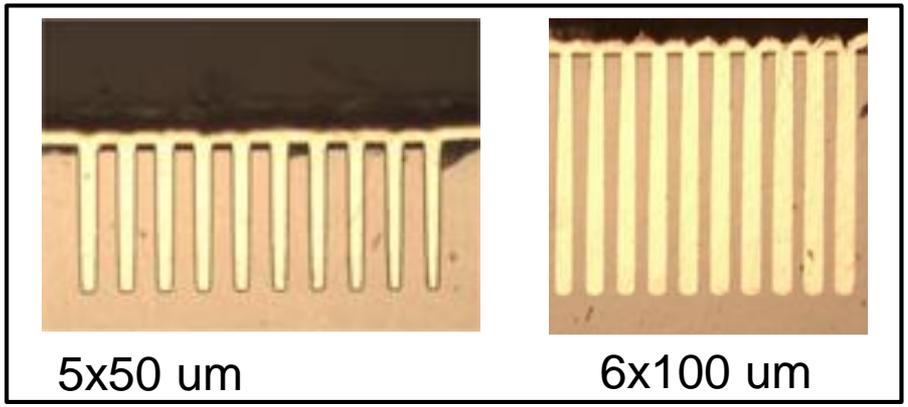
Organic additives are used to influence growth profile by locally inhibiting or catalyzing Cu deposition along via.

TSV Filling

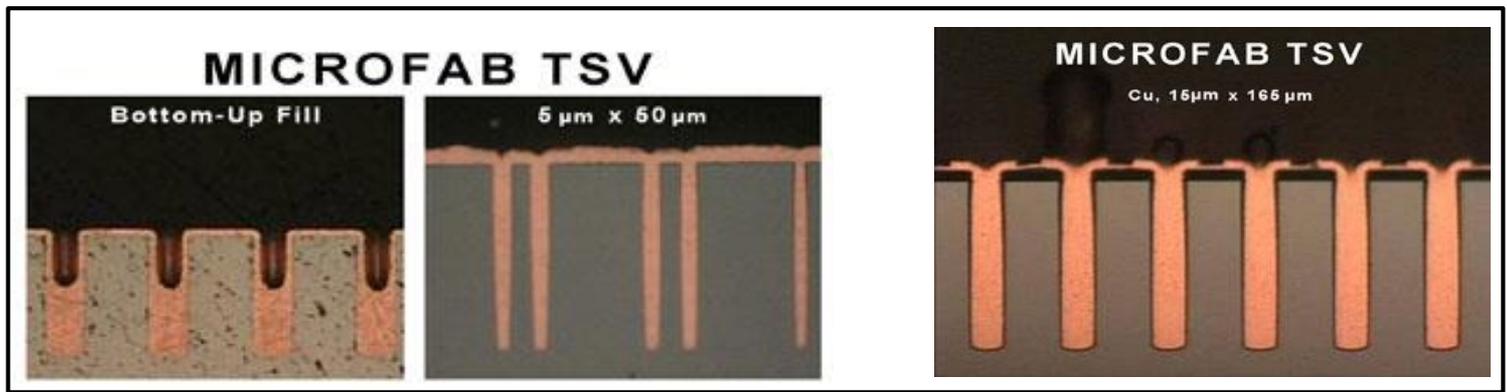
Evolution of TSV plating: from Conformal → Superconformal → Bottom up fill



10:1 TSV fill (Applied Materials)



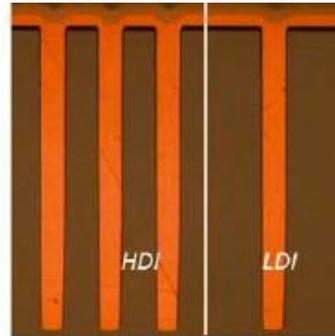
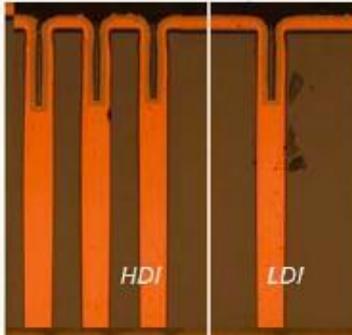
High AR TSV Fill (DOW Electronic Materials)



Bottom-Up / High AR TSV Fill (Enthone)

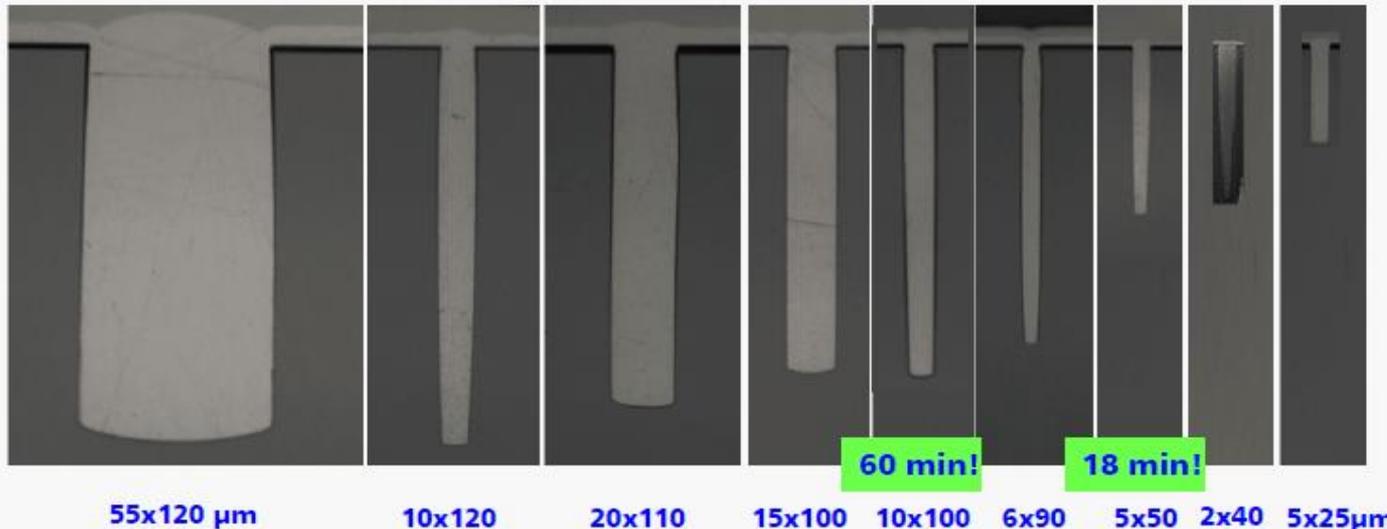
Atotech
Spherolyte III

TSV Filling- Pattern Density / Via Size



Source:
M.J. Wolf (Fraunhofer IZM ASSID),
European 3D TSV Summit, Jan. 2013

Bottom up growth for low and high pattern density 10x110 um TSVs
(Fraunhofer IZM / Atotech)

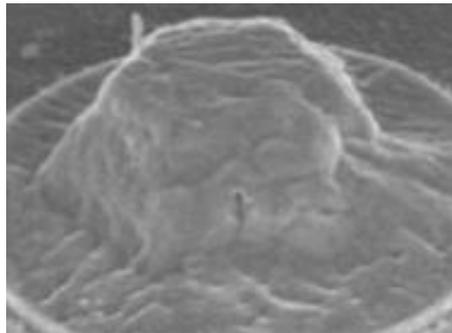


Range of TSV
dimensions and
fill times using
Spherolyte III

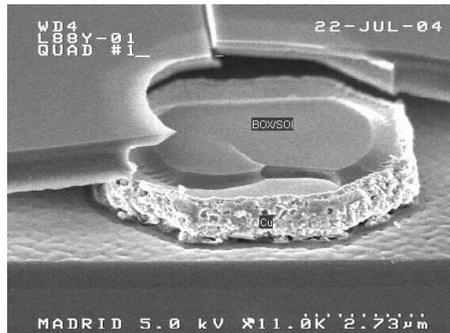
(Fraunhofer IZM /
Atotech)

Cu Protrusion / Stabilization Anneal

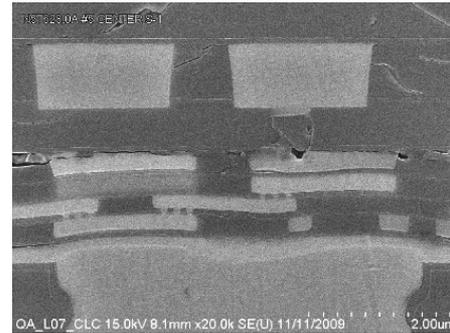
- Cu protrusion (*a.k.a.*- extrusion, pumping) is permanent swelling of TSV surface due to heating
 - Cu TSV can undergo plastic deformation due to thermal stress
 - Grain growth / microstructure change also occur
- *Stabilization anneal (typ. 300-400°C) required prior to processing subsequent layers*



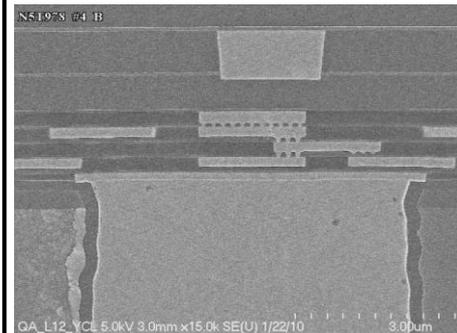
Cu hillock after anneal (IMEC)



Dielectric failure over TSV (Tezzaron)



Deformation of BEOL layers over TSV (TSMC)



Optimized ECD and anneal process (TSMC)

Overburden Removal- CMP

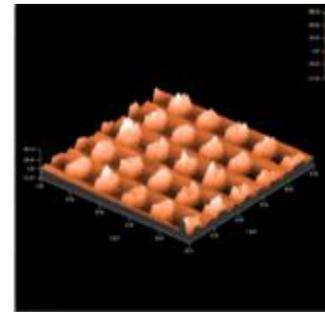
- CMP is used to remove excess ECD Cu (overburden)
- Low overburden ECD process helps limit CMP time / cost
- CMP should have high rate & uniformity across wafer

Applied Materials optimized ECD fill process – anneal and CMP

[S. Ramaswami, Handbook of 3D Integration- Vol. 3, Ch. 6]



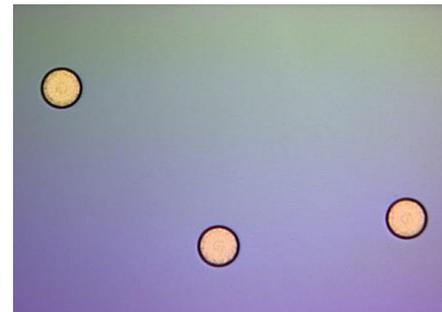
Applied Materials Reflexion CMP



Post-ECD anneal



Post CMP



Top view of Cu TSVs following CMP (RTI International)



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TSV Equipment & Process Suppliers

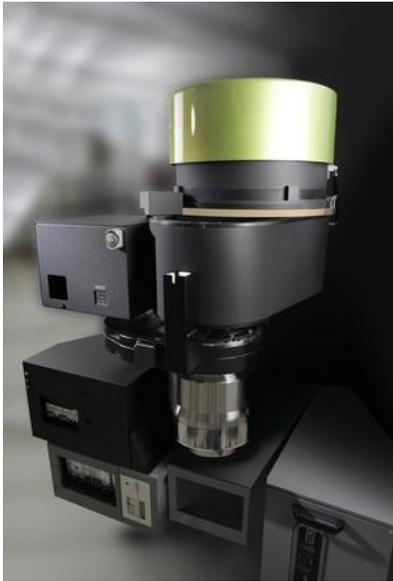
Partial list / major providers- Does not include all TSV suppliers.

(Listings are in alphabetical order)

Applied Materials

- **Centura Silvia Etch-** TSV etch
- **Producer Invia CVD-**
 - Conformal oxide for via-first / middle TSV
- **Endura Ventura PVD-**
 - TSV metallization (Ta or Ti barrier; Cu seed) to >10:1 AR
- **Raider-S ECD-** Cu fill for high AR TSV
 - Single wafer, multi chamber, integrated chemical analysis, membrane and multi-zone anode plating technology
- **Reflexion LK CMP-**
 - Copper damascene, shallow trench isolation, oxide, polysilicon, and tungsten applications

Applied Materials



Centura Silvia etch



Producer Invia CVD



Endura Ventura PVD



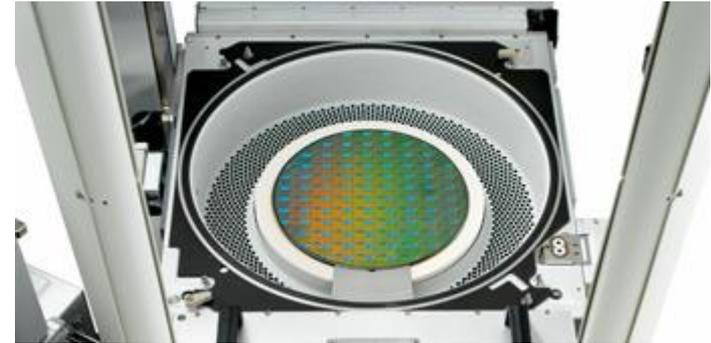
Raider-S ECD



Reflexion CMP

Lam Research

- **2300 Syndion- Etch**
 - TSV etch (DRIE)
- **Vector 3D- PECVD, PE-ALD**
 - TSV dielectric liners
- **Sabre 3D- ECD**
 - Cu TSV fill plating



Syndion- Etch



Sabre- ECD

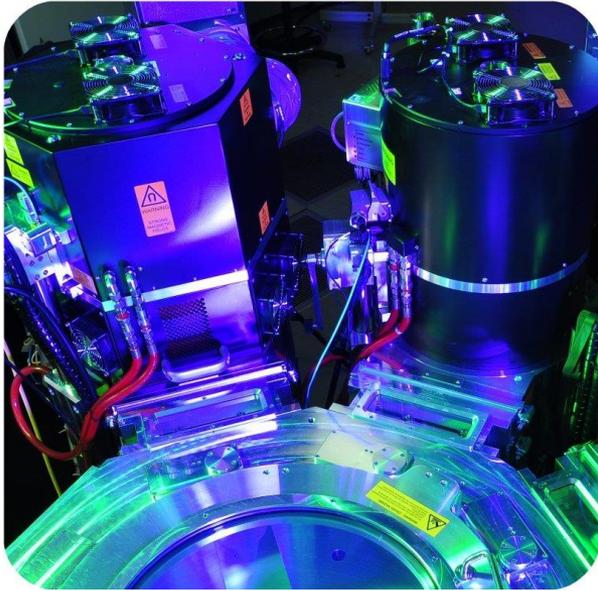


Vector 3D- CVD / ALD

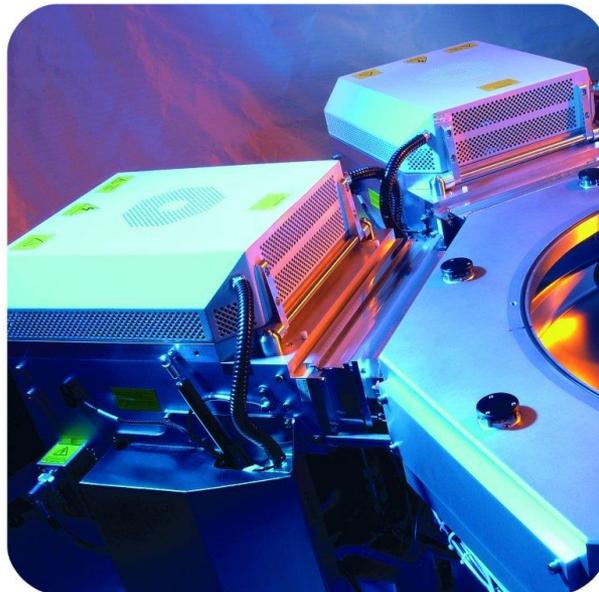
SPTS (Orbotech)

- **Omega fxP etch** with Pegasus Rapier and DSi modules:
 - TSV etch
 - Si DRIE and related oxide etches
- **Delta fxP PECVD**
 - TSV liner and other dielectric depositions
- **Sigma Advanced High Fill (AHF) PVD**
 - Ionized PVD for barrier / seed
- **Sigma C3M- MOCVD**
 - Highly conformal barrier / seed layers for high AR TSV

SPTS (Orbotech)



Omega fxP- etch with Pegasus Rapier and DSi modules



Delta fxP- PECVD



Sigma - PVD module

Tokyo Electron (TEL)

- **Stratus ECD – TSV fill**
 - TSV and various other applns (Cu pillar / RDL, bumps, fanout, etc)
- **ALD tools- high AR TSV liners**
 - **TELINDY PLUS™ IRad-** Thermal ALD (SiO₂, SiN)- 100 wafer batch
 - **NT333-** High Quality ALD SiO₂, <400 C, >100 WPH capacity
- **Appollo PVD**
 - RDL, UBM, backside metal, CMOS images sensor, etc
- **Tactras, Unity, Telius Etch tools**
- **Triase CVD**
 - Ti/TiN, W, High k gate insulating film

Tokyo Electron (TEL)



Tactras- Etch



Telindy Plus- ALD



Triase- CVD



Appollo- PVD



Stratus- ECD

ECD Materials Suppliers

Developers / suppliers of TSV plating chemistry include:

- **Atotech-** Spherolyte III
- **Dow Electronic Materials-** Interlink Copper
- **Enthone-** Microfab DVF200
- **JCU Taiwan Corp**
- **Moses Lake Industries**



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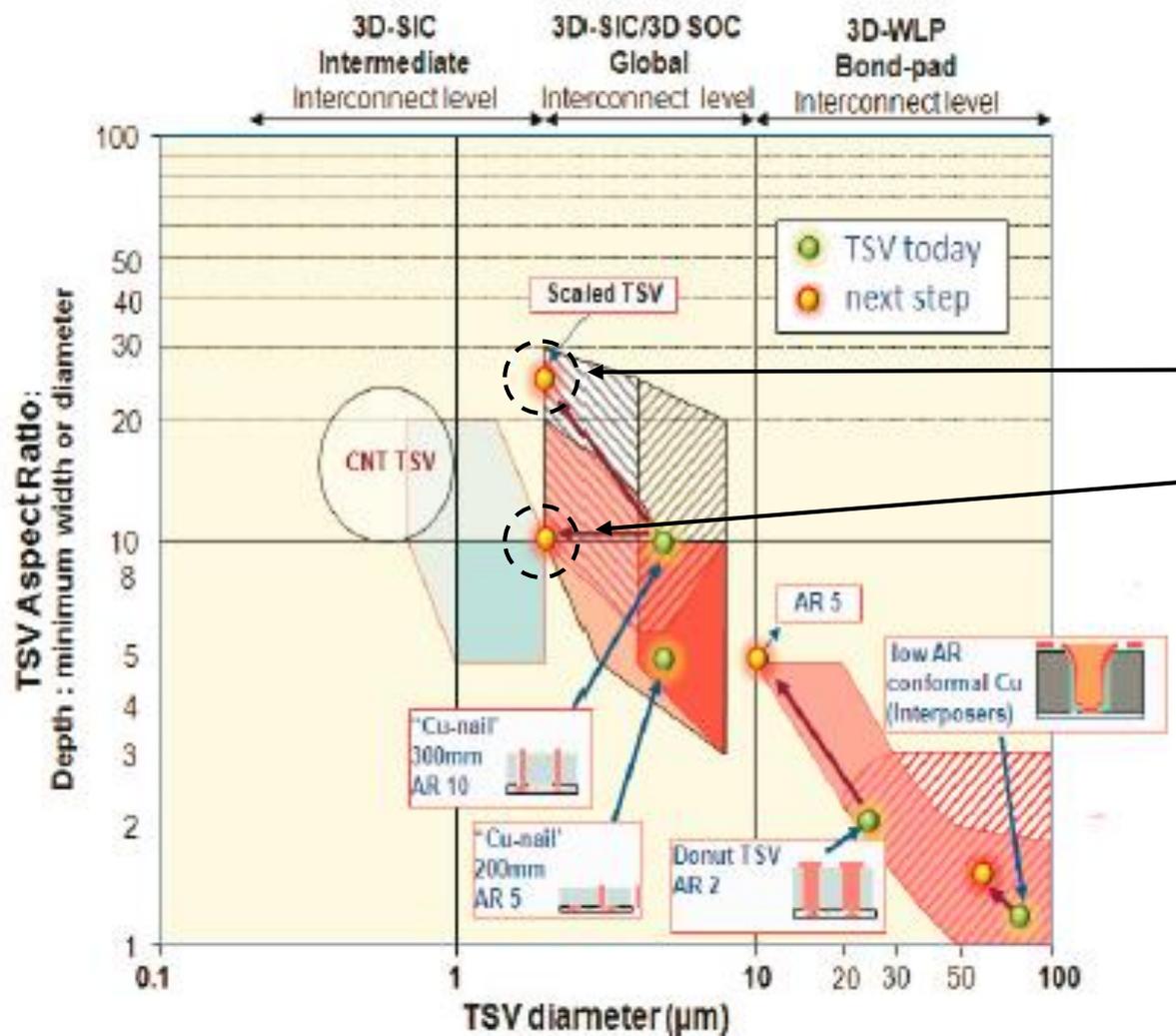
Forward Looking TSV Trends

TSV Scaling

- There are many drivers for further scaling of TSV size
 - Smaller vias =
 - Lower cost
 - Reduced reliability concern
 - Reduced keep out zone
 - Greater interconnect density
 - More highly integrated 3D applications
- ITRS roadmap for global interconnects indicates these targets for 2015-2018:
 - TSV min diameter: 2-4 um
 - TSV aspect ratio: 10:1-20:1

[REF- INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS), 2011 EDITION- INTERCONNECT]

TSV Scaling



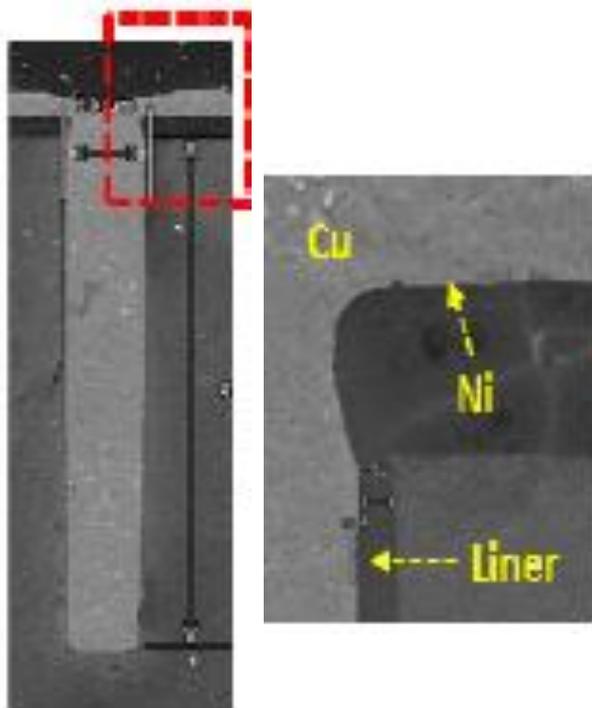
IMEC has indicated TSV scaling to reach diameters of 2-3 μm, AR of 10:1-25:1

(around transition from Global to Intermediate Interconnect level)

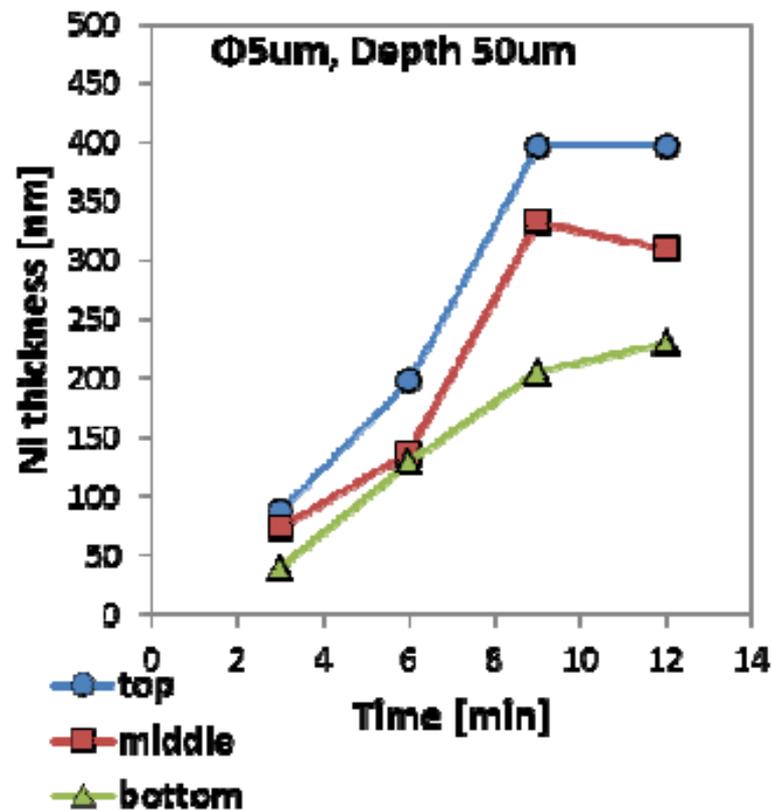
High AR TSV Materials and Processes

- Further TSV scaling will mean higher aspect ratio, challenging the current deposition & fill methods
 - PVD barrier / seed and some CVD dielectrics may reach limits
- Alternative processes and materials are emerging for possible use in high AR TSVs (e.g., 3x50 um- 17:1)
 - ALD (dielectric, barrier, seed)
 - MOCVD (barrier, seed?)
 - Wet processes (ECD / ELD - dielectric, barrier, seed)
 - New Cu ECD via filling chemistries and methods

High AR options- electroless barrier (Tohoku Univ.)



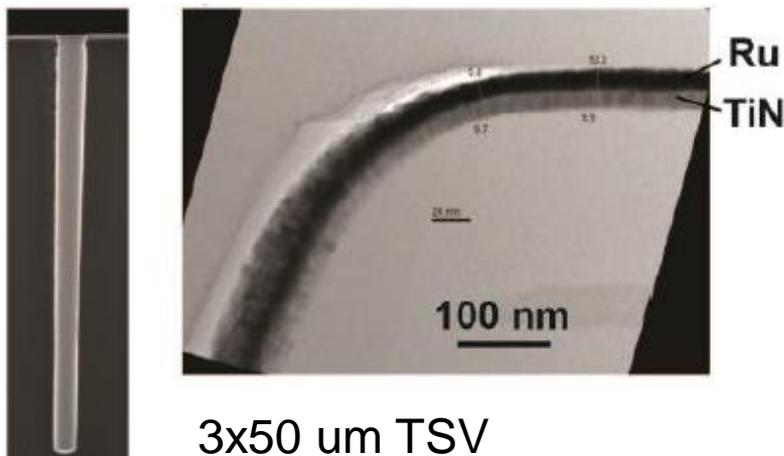
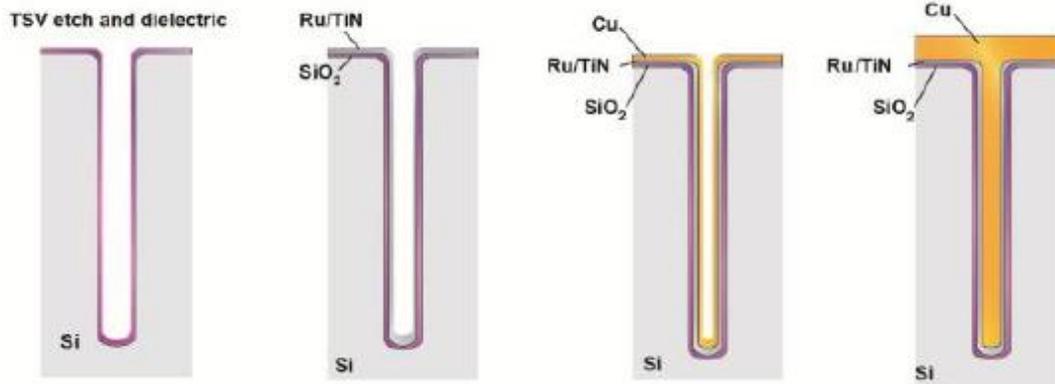
Electroless Ni barrier-
Tohoku Univ.
(2014 3DIC conference)



Conformality improved to ~50%

High AR options- ALD / ELD barrier & seed (IMEC / Tohoku)

(a) I. Dielectric II. Liner/Barrier ALD III. Seed ELD IV. Filling



3x50 um TSV

High AR TSV process
(e.g., 3x50 um, 17:1)

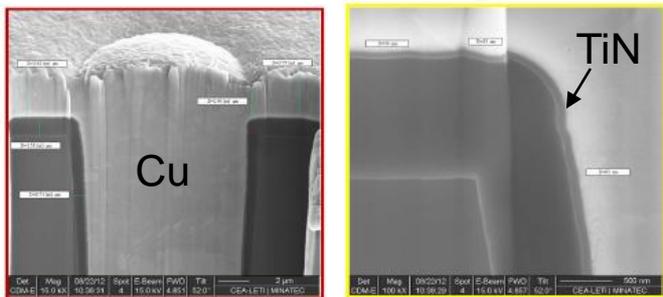
IMEC / Tohoku Univ.
(2014 3DIC conference)

Proposed flow:

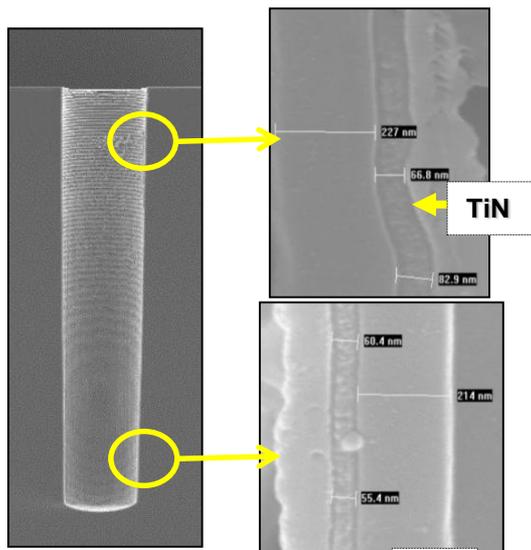
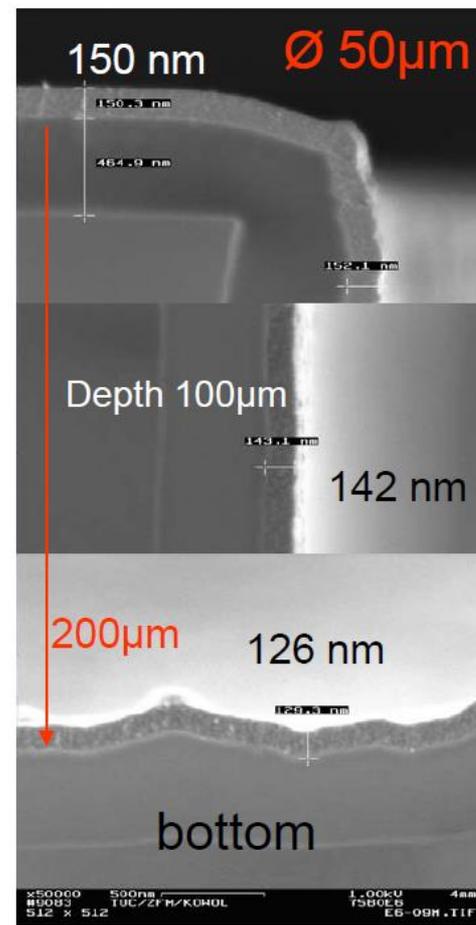
- CVD SiO_2
- ALD TiN barrier + ALD Ru liner (catalyst for Cu seed)
- Electroless deposition (ELD) Cu seed

High AR options- MOCVD barrier

MOCVD TiN barrier- SPTS



MOCVD TiN barrier- Fraunhofer ENAS



**<200°C MOCVD TiN:
80% coverage in 5.3:1 via**

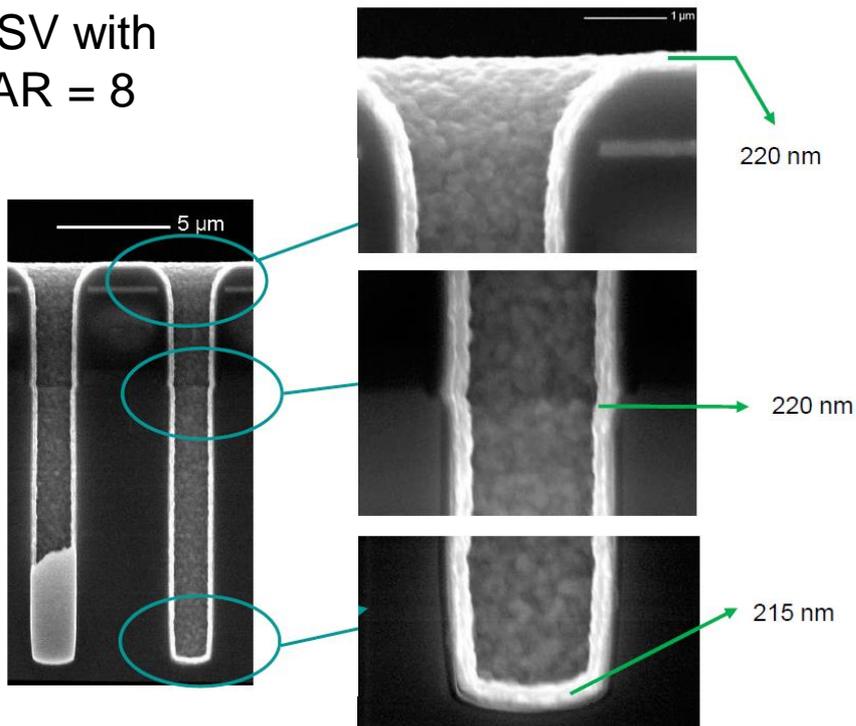
84% conformal (4:1 via)

High AR options- MOCVD Cu

- MOCVD Cu is nearly 100% conformal and extends to very high AR
- Specialized process- cost and throughput limit production use

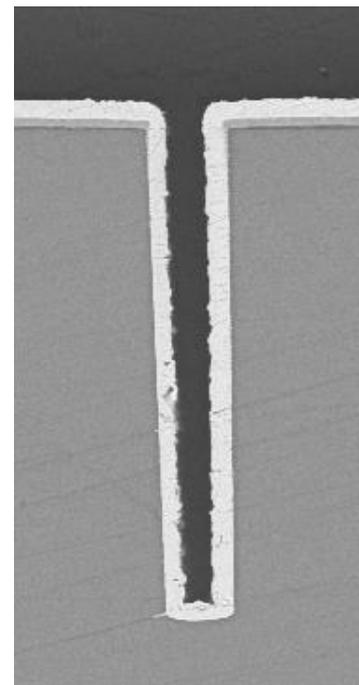
MOCVD Cu- Fraunhofer ENAS

TSV with
AR = 8



98% conformal

MOCVD Cu- RTI International



4x26 um
(AR=6.5)

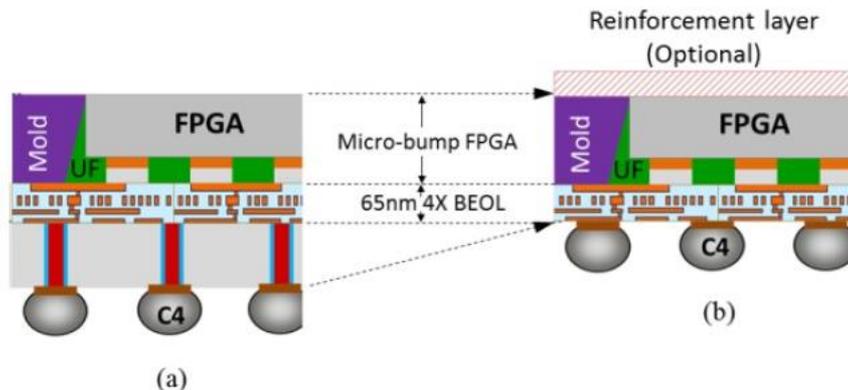
~100% conformal

Competing Approaches to TSV Interposer

- As TSV cost concerns continue, many groups are looking at mold-based substrate alternatives to TSV

Example:

- Xilinx and SPIL (IMAPS 2014 in San Diego)
“Cost effective, high performance 28nm FPGA with new disruptive Silicon-less Interconnect Technology (SLIT)”
- This approach is for FPGA integration on 4-layer 65nm interconnect (same as prior Si interposer), but eliminates TSVs and all Si



Source: Solid State Technology (electroiq.com)



3D Architectures for Semiconductor Integration and Packaging

3D ASIP December 10-12, 2014, Burlingame, California

Acknowledgments

Acknowledgments

Special thanks for consultation and data contributions to this talk:

- SPTS: David Butler, Jay Chess, Andrew Tucker
- Phil Garrou (Microelectronics Consultants of NC)

Acknowledgment of technical content originating from:

- IMEC, Fraunhofer (IZM, ENAS), ASET, TSMC, Tezzaron, Xilinx, IBM, DRS, Toshiba, Yole Développement, Tohoku University
- Applied Materials, LAM, SPTS, TEL, ULVAC
- Atotech, DOW, Enthone