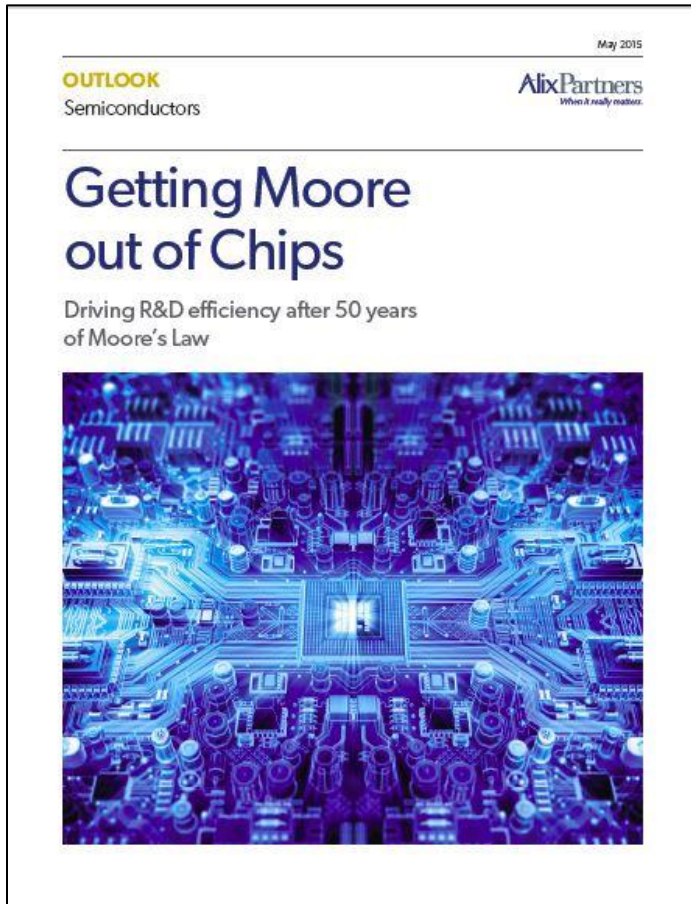

How 2.5/3D Technologies Will Shake Up the Semiconductor Supply Chain and Cost Structure

Scott Jones
Alix Partners
Director & Semiconductor Practice Lead

Enterprise Improvement
Financial Advisory
Information Management
Leadership & Organizational Effectiveness
Turnaround & Restructuring

AlixPartners
When it really matters.

Recent AlixPartners Publication: Getting Moore Out of Chips



Pressure on Profitability is Coming from Multiple Sides:

- Revenue Growth is Slowing Across the Industry
- R&D Costs are Increasing Significantly From Generation to Generation
- Fewer Semiconductor Companies Can Support Leading Edge Designs
- Increasing R&D Spending Does Not Necessarily Lead to Higher Profits
- Companies that have a Disciplined Process for Aligning R&D Investment with Market Opportunities Demonstrate Higher Levels of Profitability

The industry is going through consolidation at an unprecedented rate as a result of slower growth and increasing costs of R&D and manufacturing

Traditional Topics for 3D/2.5D and TSV

TSV Process Definition

How do we take 2.5D and 3D to HVM?

What are the Process Tools Required

Tool and Materials Availability

- Wafer Thinning, Temporary Bonding and Carriers

Yield/Test Challenges

Which Stacking Option is Best:

- Interposer, W2W, D2D, D2W

Performance Benefits of 2.5D and 3D?

What is the cost gap?

Supply Chain Impacts

Industry Headlines

14nm FinFETs are here!

But their late...

And they're expensive...

10nm is likely late as well...



EUV is making progress!

But will not be available for 10nm ramp...

Doubts remain about it's availability on 7nm...



And 450mm... No news is not good news.



Meanwhile in the world of 3D...

More and More Applications of 3D Integration in the Market

PASCAL

- NVLink 5 to 12X PCIe 3.0
- 3D Memory 2 to 4X memory BW & size
- Module 1/3 size of PCIe card

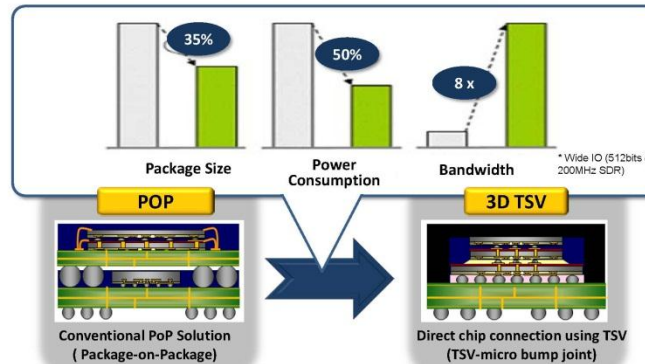




TSV (Through Silicon Via) Technology

Current Application Sweet Spot in Samsung

- 3D TSV : Logic and Wide IO Memory direct stacking with TSV



Smart & Innovative Foundry Solution 



THE WALL STREET JOURNAL.



Sony Plans \$3.6 Billion Stock, Bond Offering

Japanese electronics maker plans to invest in image sensor business.



What are the questions we ask on behalf of our clients?

Are we measuring the cost gap correctly?

- Use a full fab model versus isolated flows
- Quantify supply chain impact

Can the 2.5D/3D community close the gap?

Will the end of scaling close the gap for us?

- Litho capacity as a driver

How can modularity impact the supply chain?

How do drivers in end market growth shift our focus?

Do end market product cycles make 2.5D and 3D more attractive?

How much does standardization matter?

Think Like a Fab Owner

How does this impact my capital investment?

What is the re-use and do I need new tools?

If so, is there floor space?

What mix optimizes my margins?

Do I take wafer starts away from existing products and customers?

This doesn't just apply to fabs though. Consumers of leading edge capacity must understand these questions because it's their products that fill the fabs on the leading edge.



The Building Blocks for Fab Cost Modeling

Create the basic building blocks for ongoing analysis to drive business value

Understanding of Manufacturing Cost Drivers

- Total Cost of Ownership Models for tools and hourly cost to operate
- Throughput assumptions for all operations required to generate full wafer flows
- Allocation Models for complex fixed cost structures at detailed levels
- Assignment of Maintenance Costs and Modeling for Tool Uptime and Availability
- Ability to extract and leverage MES data to validate time on machine assumptions

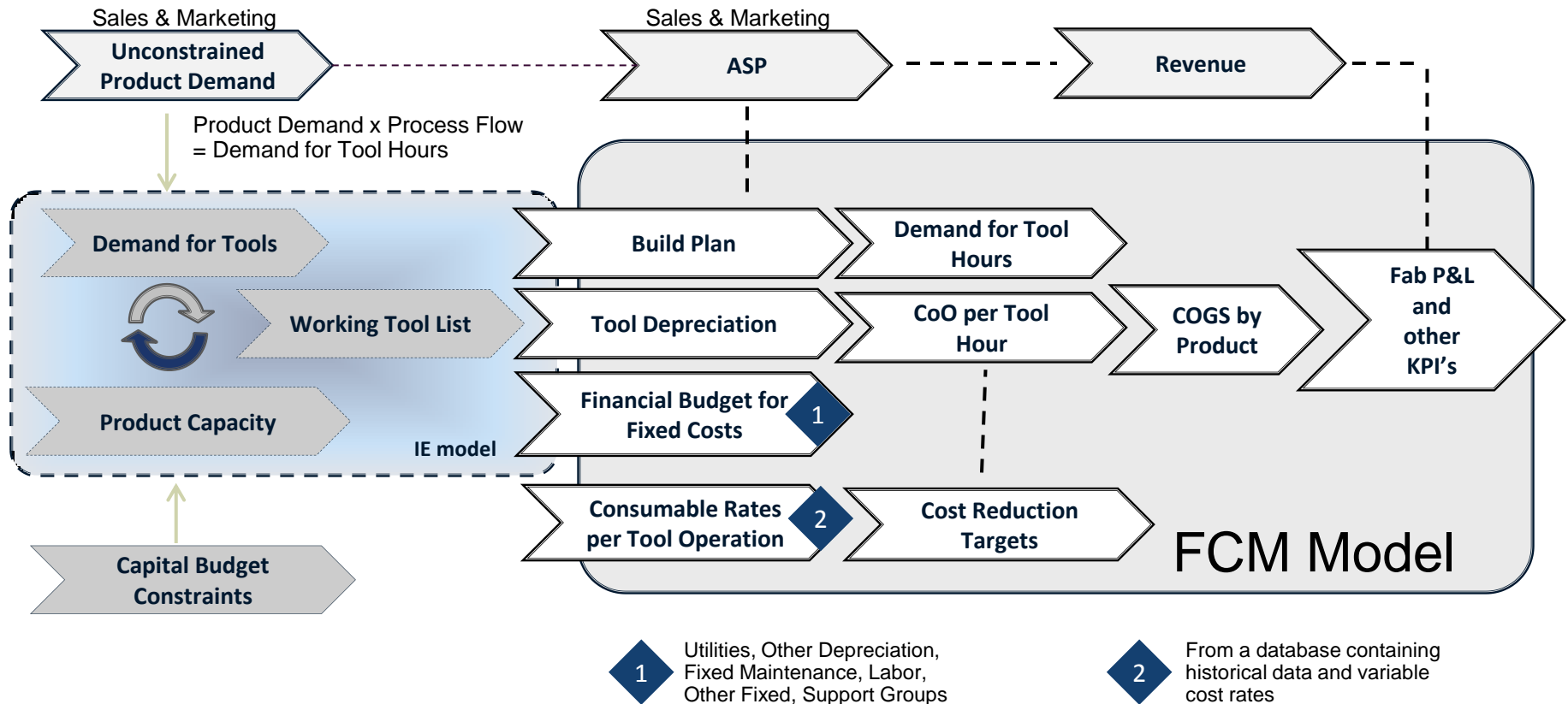
Providing Tools to Support Better Decision Making

- Ability to create dynamic models to value options and sensitivity of manufacturing decisions
 - Being able to determine when technology transitions should happen
 - EUV
 - 2.5D/3D/TSV
 - Memory
-

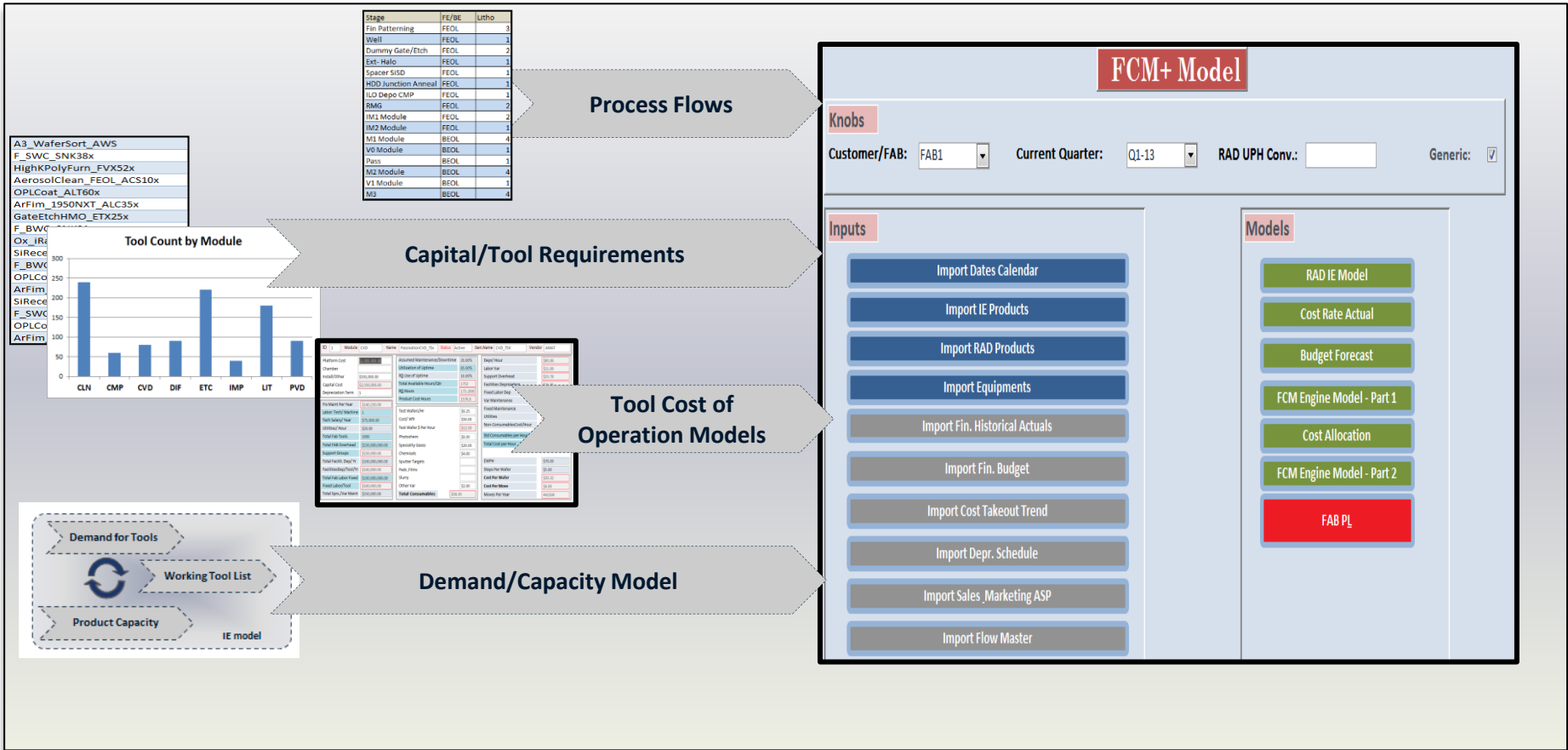
Architecture of the Fab Cost Model

FCM Inputs: Sales, Pricing, TD, IE, Site Finance

FCM leverages existing processes to lower effort required to maintain rolling forecast at the Fab level for profitability tied to the Executive S&OP Forecast Monthly



Key Components of Cost Modeling



A full fab view is necessary to understand the downstream impacts of integrating new technologies into the HVM environment

Total Cost of Ownership Model for Each Tool in the Fab

The TCO Model allows for multiple inputs for Tool Cost, Throughput, Performance, Fab Cost Structure and Application to Process Flow

Capital and Installation Costs

Fab Overhead:
Utilities
Labor
Facilities Cost

Maintenance Spending per Financial Periods

Variable Costs:
Consumables - Gases, Chemicals, etc.

Each TCO Model is included in the VFM

Uptime Availability and Utilization

Units per Hour to determine through up the step for the flow

Steps required for process flow

ID	1	Module	CVD	Name	PassivationCVD_75x	Status	Active	Gen.Name	CVD_75X	Vendor	AMAT
Platform Cost											
Chamber											
Install/Other											
Capital Cost											
Depreciation Term											
Fix Maint Per Year											
Labor: Tech/ Machine											
Tech Salary/ Year											
Utilities/ Hour											
Total Fab Tools											
Total FAB Overhead											
Support Groups											
Total Facilit. Dep/ Yr											
FacilitiesDep/Tool/Yr											
Total Fab Labor Fixed											
Fixed Labor/Tool											
Total Sprs./Var Maint											
Assumed Maintenance/Downtime											
Utilization of Uptime											
RD Use of Uptime											
Total Available Hours/Qtr											
RD Hours											
Product Cost Hours											
Test Wafers/Hr											
Cost/ Wfr											
Test Wafer \$ Per Hour											
Photochem											
Speciality Gases											
Chemicals											
Sputter Targets											
Pads_Films											
Slurry											
Other Var											
Total Consumables											
Depr/ Hour											
Labor Var											
Support Overhead											
Facilities Depreciation											
Fixed Labor Dep											
Var Maintenance											
Fixed Maintenance											
Utilities											
Non-ConsumablesCost/Hour											
Std Consumables per Hour											
Total Cost per Hour											
EWPH											
Steps Per Wafer											
Cost Per Wafer											
Cost Per Move											
Moves Per Year											

FCM+ Model	
Inputs	Models
Import Status Calendar	Import Model
Import B. Products	Cost Rate Actual
Import B. Products	Bridge Forecast
Import Components	FCM Engine Model - Part 1
Import File: Historical Actuals	Cost Allocation
Import File: Budget	FCM Engine Model - Part 2
Import Cost Internal Demand	FAB PL
Import Date: Schedule	
Import Sales: Marketing ATP	
Import Flow Monitor	

TCO Example Example – Qualifying a Tool for TSV

Example: Usage Profile

Having a tool split time between traditional flows and TSV flows will change the hours required and the potential uptime of the tool

ID	1	Module	CVD	Name	PassivationCVD_75x	Status	Active	Gen.Name	CVD_75X	Vendor	AMAT
Platform Cost					\$2,000,000.00						
Chamber											
Install/Other					\$550,000.00						
Capital Cost					\$2,550,000.00						
Depreciation Term					5						
Fix Maint Per Year					\$140,250.00						
Labor: Tech/ Machine					1						
Tech Salary/ Year					\$75,000.00						
Utilities/ Hour					\$20.00						
Total Fab Tools					1000						
Total FAB Overhead					\$150,000,000.00						
Support Groups					\$150,000.00						
Total Facilit. Dep/ Yr					\$100,000,000.00						
FacilitiesDep/Tool/Yr					\$100,000.00						
Total Fab Labor Fixed					\$100,000,000.00						
Fixed Labor/Tool					\$100,000.00						
Total Sprs./Var Maint					\$350,000.00						
Assumed Maintenance/Downtime					20.00%						
Utilization of Uptime					85.00%						
RD Use of Uptime					10.00%						
Total Available Hours/Qtr					1752						
RD Hours					175.2000						
Product Cost Hours					1576.8						
Test Wafers/Hr					\$0.25						
Cost/ Wfr					\$50.00						
Test Wafer \$ Per Hour					\$12.50						
Photochem					\$0.00						
Speciality Gases					\$20.00						
Chemicals					\$4.00						
Sputter Targets											
Pads_Films											
Slurry											
Other Var					\$2.00						
Total Consumables					\$38.50						
Depr/ Hour					\$80.86						
Labor Var					\$11.89						
Support Overhead					\$23.78						
Facilities Depreciation					\$15.85						
Fixed Labor Dep					\$15.85						
Var Maintenance					\$55.49						
Fixed Maintenance					\$22.24						
Utilities					\$20.00						
Non-ConsumablesCost/Hour					\$245.97						
Std Consumables per Hour					\$38.50						
Total Cost per Hour					\$284.47						
EWPH					\$70.00						
Steps Per Wafer					\$5.00						
Cost Per Wafer					\$20.32						
Cost Per Move					\$4.06						
Moves Per Year					441504						

This change in usage profile for a tool group would be fed into the full Fab P&L profile to see how it affects the total throughput of the fab and its total revenue generating capability

Knobs

Customer/FAB: FAB1 Current Quarter: Q1-13 RAD UPH Conv.: Generic: [x]

Inputs

- Import Dates Calendar
- Import IE Products
- Import RAD Products
- Import Equipments
- Import Fin. Historical Actuals
- Import Fin. Budget
- Import Cost Takeout Trend
- Import Depr. Schedule
- Import Sales Marketing ASP
- Import Flow Master

Models

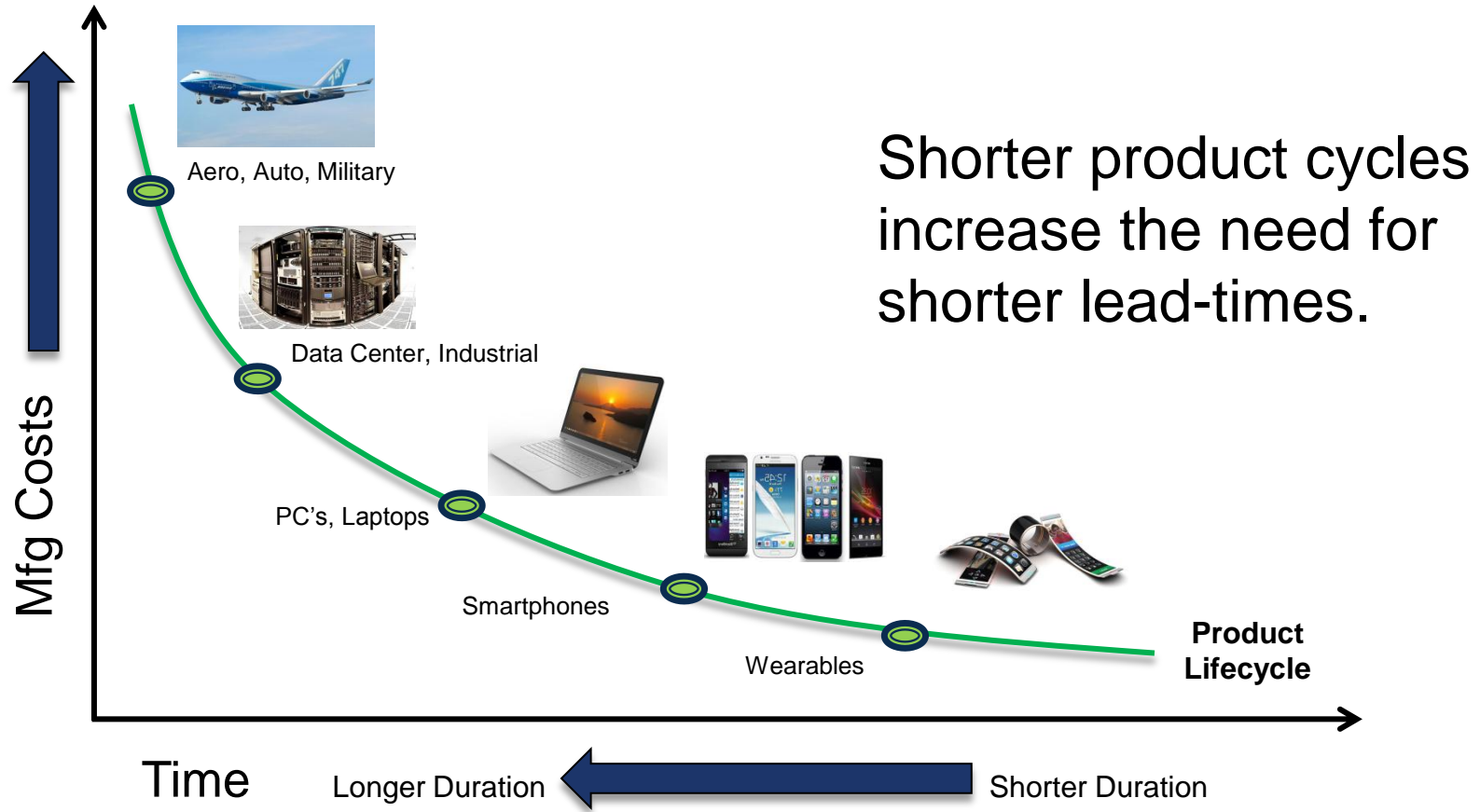
- RAD IE Model
- Cost Rate Actual
- Budget Forecast
- FCM Engine Model - Part 1
- Cost Allocation
- FCM Engine Model - Part 2
- FAB P/L

Benefits of 2.5D/Interposer and 3D Approaches

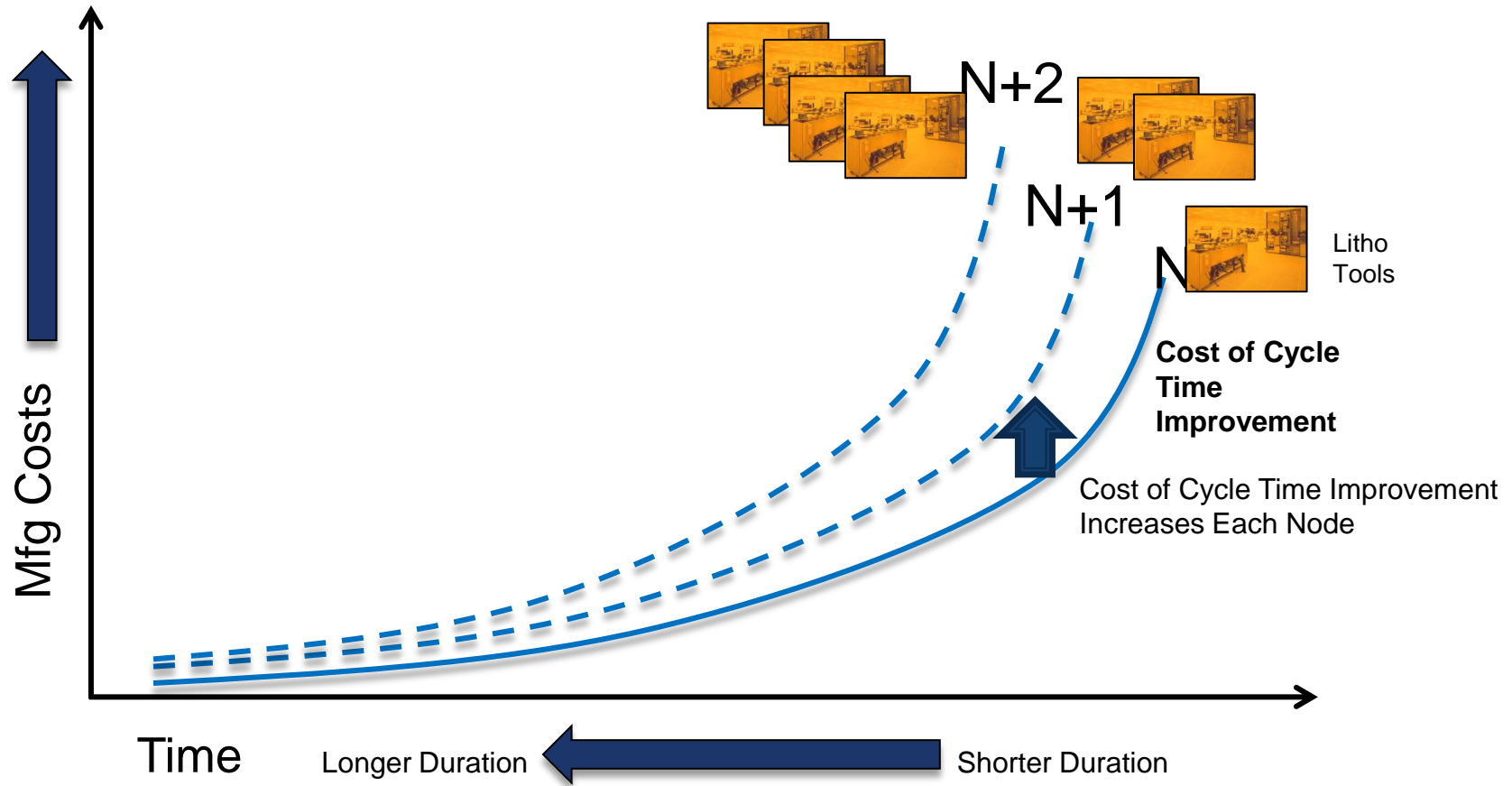
Considerations:

- Lower Exposure to Leading Edge Capacity Issues
- Segregation of scalable parts of the chip versus non-scalable
- Equipment Utilization- Cycle Time Impact
- Incremental Capital Impact
- Supply Chain Impacts- Flexibility- Delayed Differentiation
- Design Costs, Integration, Pre-Si Validation, Post-Si Validation

Optimization of Cycle Time v. Cost Changes Based on End Market and Technology

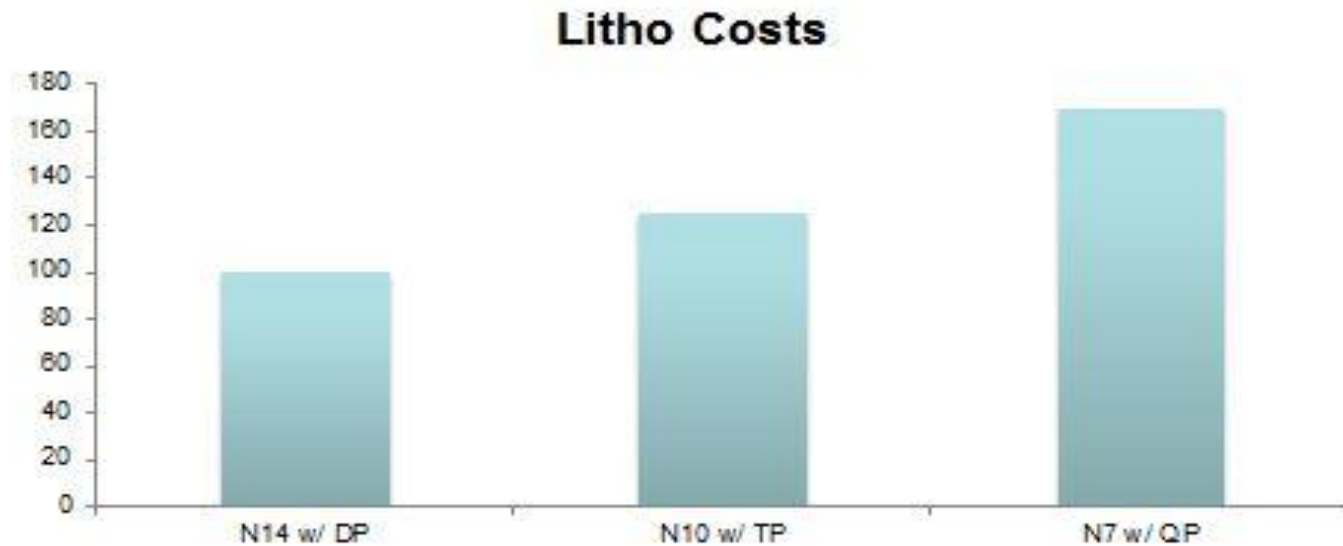


Cost of Improving Cycle Time Increases Dramatically with Multi-Patterning



It's not just litho... Other challenges: Single Wafer Cleans, ALD, Embedded SiGe

Leading Edge Exposure to Rapidly Rising Lithography Costs



**Lithography costs are increasing at faster rates due to multi-patterning.
2.5/3D can lower exposure to leading edge Lithography requirements**

Reducing Lead Times- Why do we care?

Long Cycle Time = Inventory Risk

Semiconductor Industry Inventory Turnover Ratio is ~4.5.

25%-35% of Capital is spent to reduce cycle time, not for additional capacity.

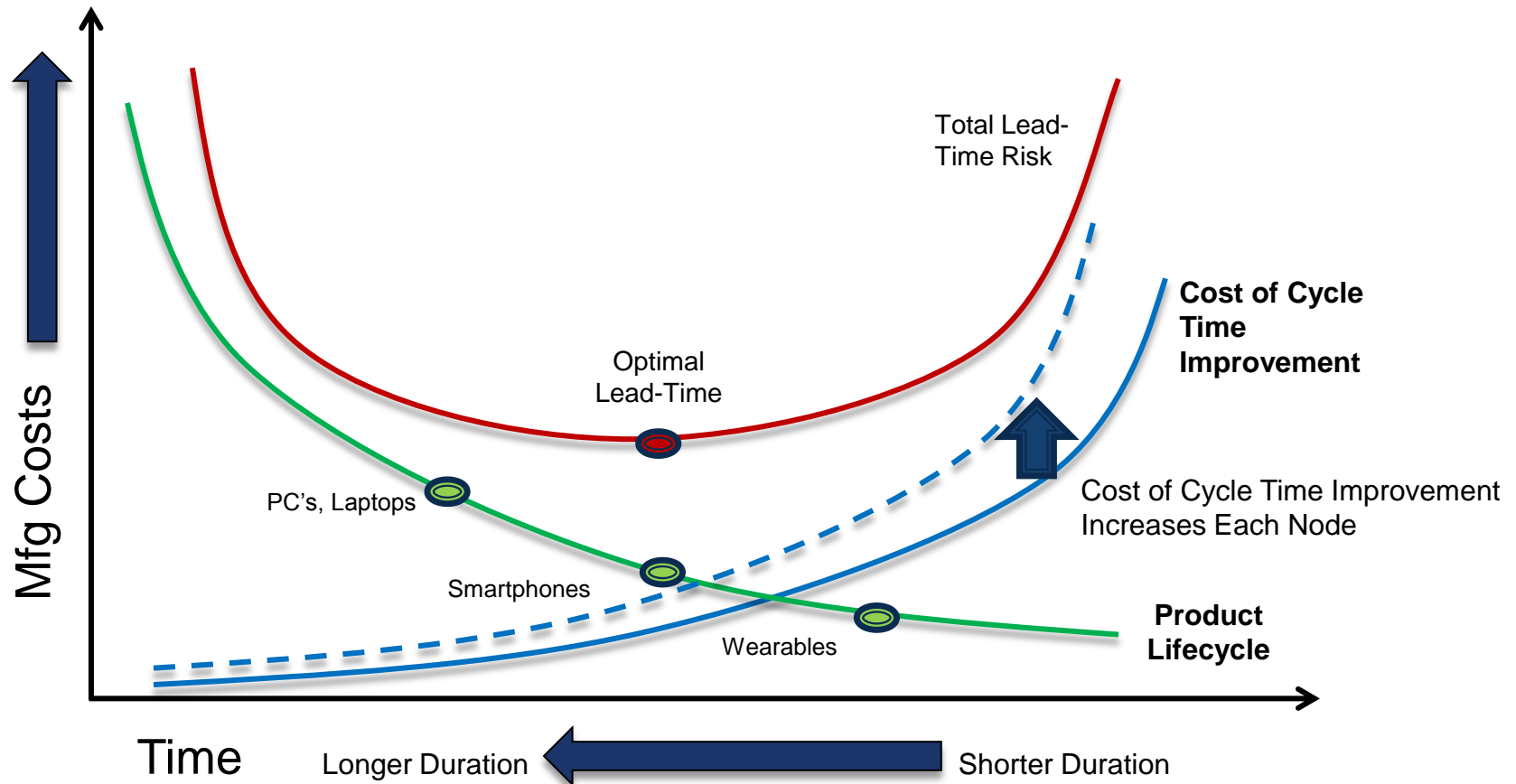
- The S&P is ~8.5

Intel called their inventory “Brown Bananas”

- As soon as it came off the line, it started going bad

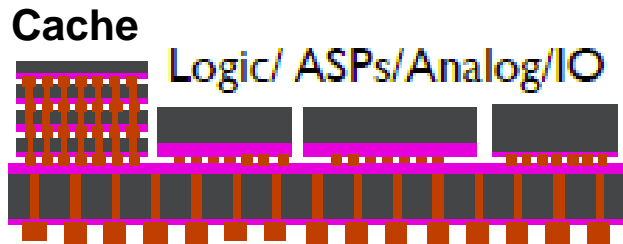


Optimization of Cycle Time v. Cost Changes Based on End Market and Technology



HVM Example- Interposer

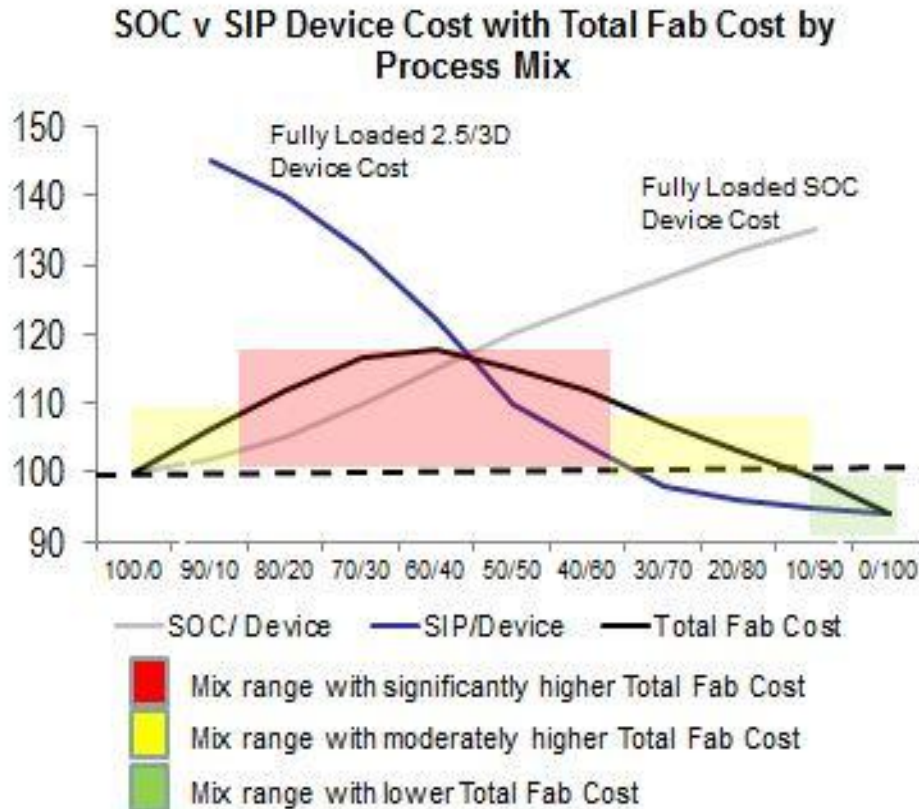
- 4 Different SKU's on 14nm FinFET
- 4 Different Designs versus TSV/2.5D Approach



Example of 4 Products Requiring 14nm Logic

- High End SOC – 4+ Multi Core Logic + ASIC and L2 & L3 Cache
- Mid-Tier Dual Core with ASIC
- Mid-Tier Dual Core Logic with L2 Cache
- Low End- One Core and & L1 Cache

Fab total costs at various loading mix between SOC and 2.5/3D processes



- Above 70% mix to 2.5/3D devices the fab can tolerate higher costs by offsetting supply chain impacts although SOC device costs would be above tolerance levels for fabless companies
- Above 90% mix to 2.5/3D devices the total fab costs are lower and device costs lower at the silicon level
- Below 50% mix to 2.5/3D the device cost is too high to support all but the extreme high-end applications

HVM Example- Interposer

4 Different SKU's on 14nm FinFET

4 Different Designs versus TSV/3D Approach

	Fab 1- SOC	Fab 2- SIP	
Capacity	50k month	50k month equivalent	Lower capital due to less exposure to 14nm process
Die	8mm x 8mm	Multi-Die on 65nm Interposer	Digital/Analog, Cache on 65nm Interposer w/ TSVs
Finished Products	~120m finished products	~120m finished products	Roughly same assuming similar yield
Silicon Cost	\$5.42 per device	\$4.97 per device	8% Lower Silicon Cost

Source: AlixPartners Research

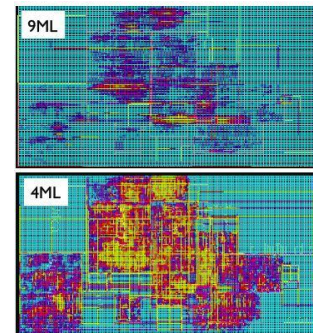
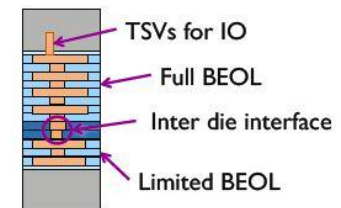
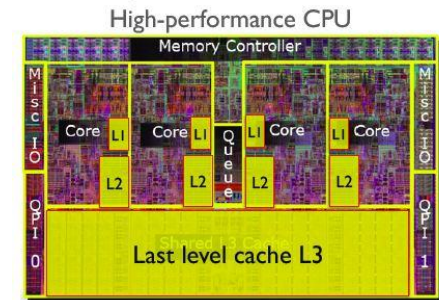
3D Integration Example: W2W Heterogeneous Die

Assumptions for 28nm 9ML Wafer Cost:

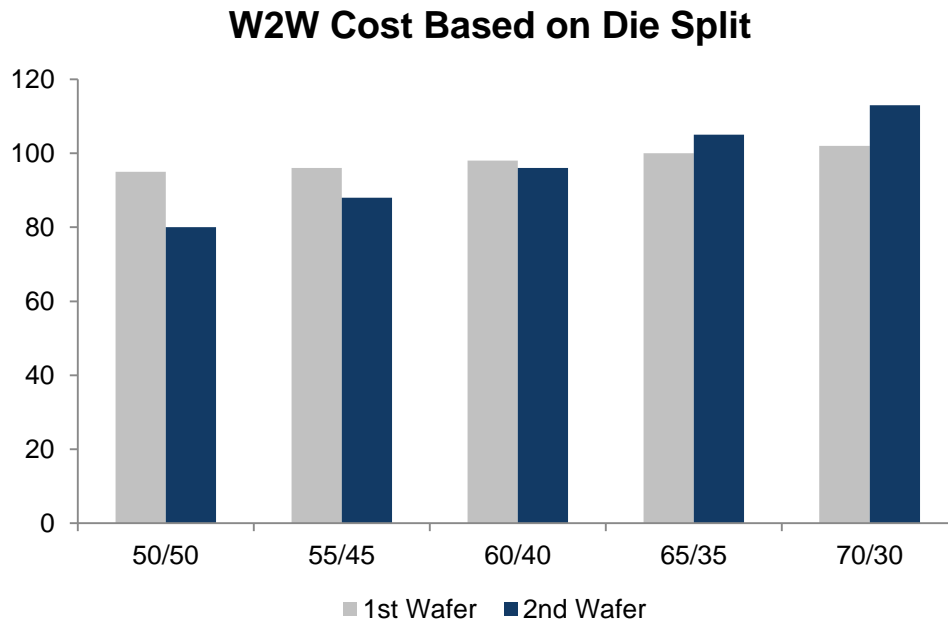
- 48% FEOL
- 42% BEOL
- 10% Metrology

W2W Integration +15% of Wafer Cost

- 9 Metal Layer for 1st Wafer
- 4 Metal Layer for 2nd
- Same yield as for 2D Wafers



Preliminary Cost Model Output Shows Cost Savings Potential for W2W Heterogeneous Die



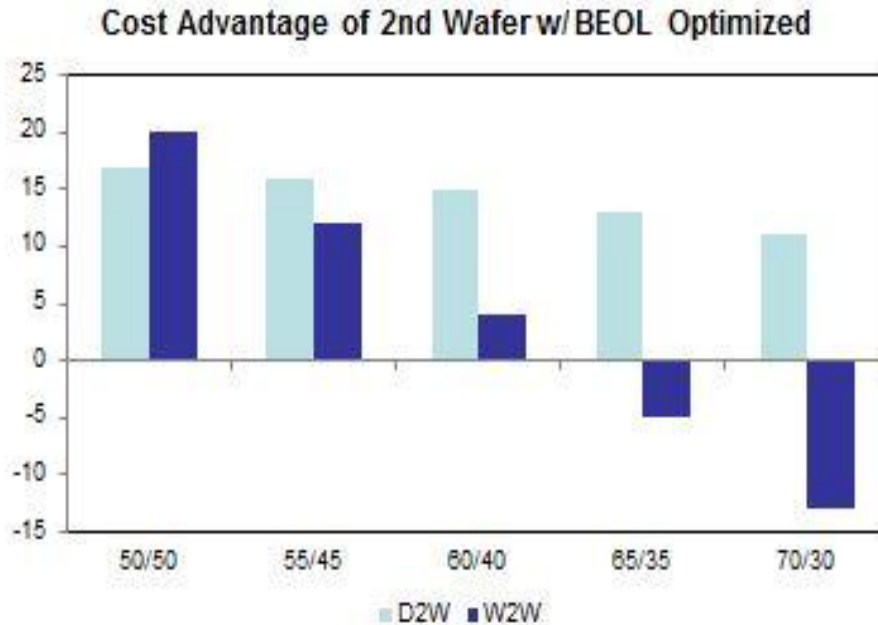
At 50/50 ratio of die on 1st Wafer to 2nd Wafer there is up to 20% Reduction on 2nd Wafer based on lower BEOL costs and lower capital required

No cost advantage when ratio of die size is 65/35 or worse

No cost savings considered for lesser die size based on fewer repeaters

Die size ratio of 1st and 2nd wafer is biggest driver of potential cost savings.

Preliminary Cost Model Output Shows Cost Savings Potential for D2W Heterogeneous Die



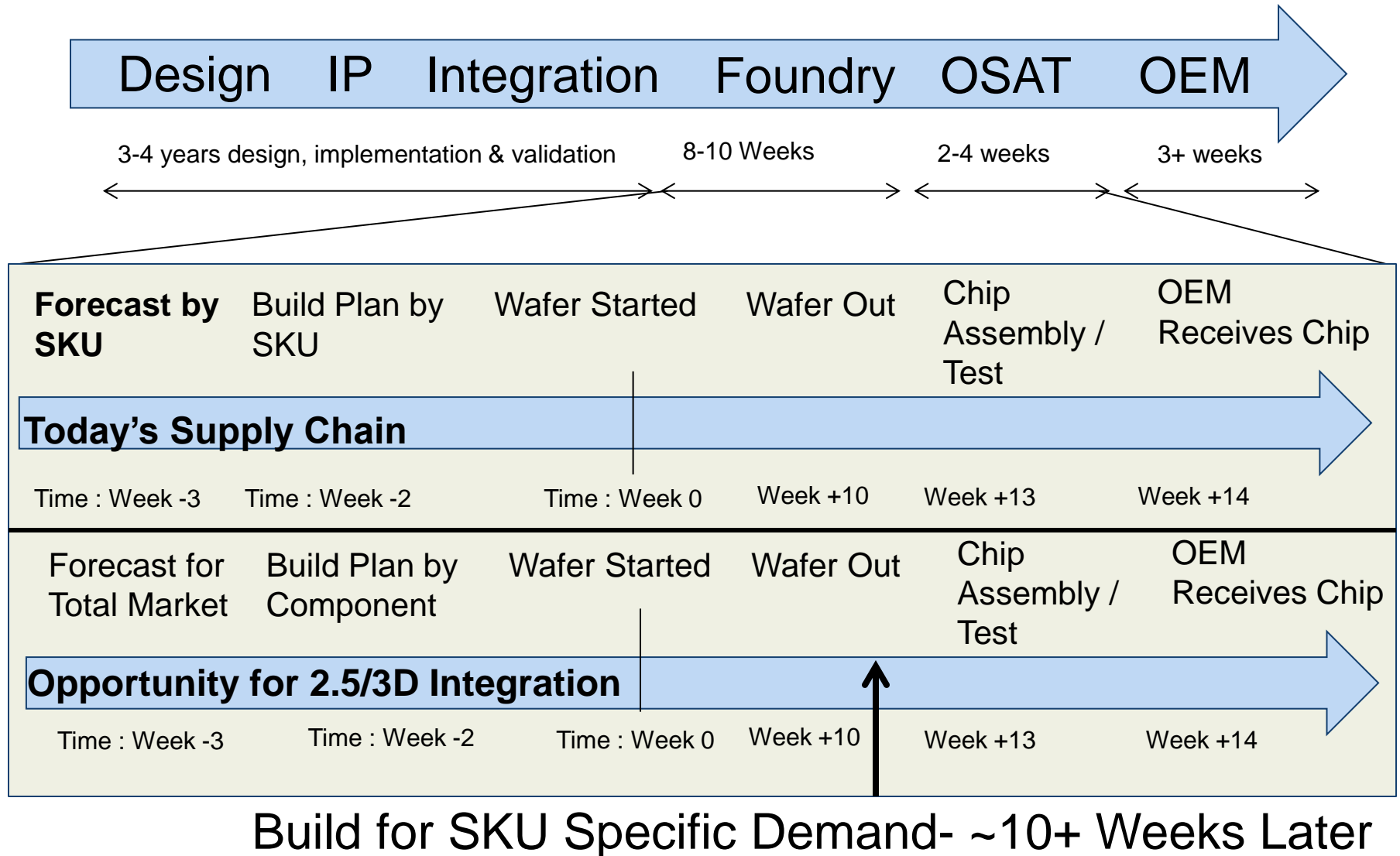
Assumes 95% yield per die area and 98% yield for D2W process

Cost advantage of 50/50 die split is not as high with D2W

D2W does have advantage as die split ratios diverge from 50/50

D2W approach reduces the sensitivity to the ratio of die size between wafer one and wafer two

Semiconductor Value Chain



Concluding Thoughts...

- When thinking of the value of 2.5/3D TSV, think **BIG!**
- Understand the impact on the entire fab of your manufacturing partner.
- Work with your Supply and Operational Planning group to understand the benefit of supply chain optimization
- Engage with finance throughout the entire process. They're not just there to keep you from doing the things you want to do!
- Leverage total cost of ownership models as a tool to differentiate your offering and quantify the value.
- For years industry cost trends moved away from 2.5/3D applications and now it's moving towards it. Be ready to meet it.