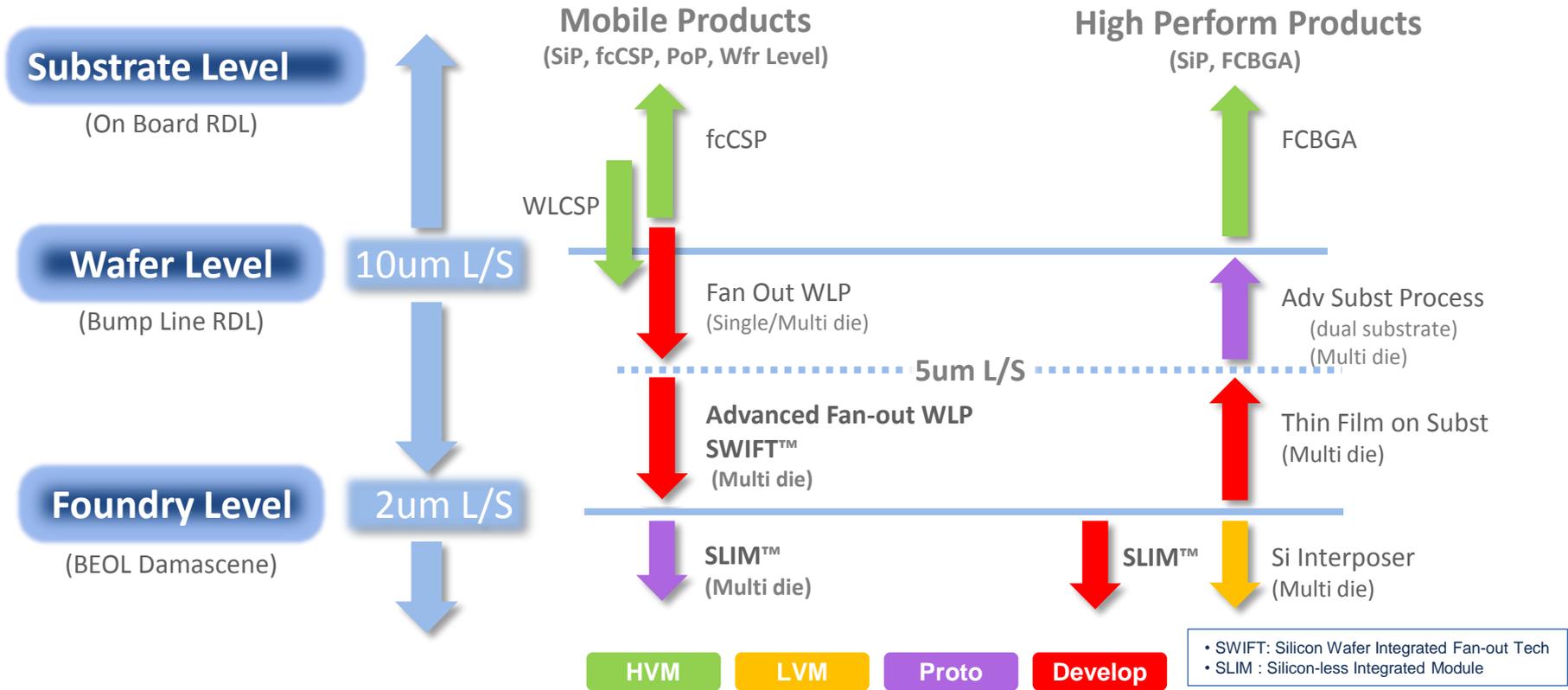


Amkor's SLIM & SWIFT Package Technology

Ron Huemoeller | SVP Advanced Package Technology Develop & IP

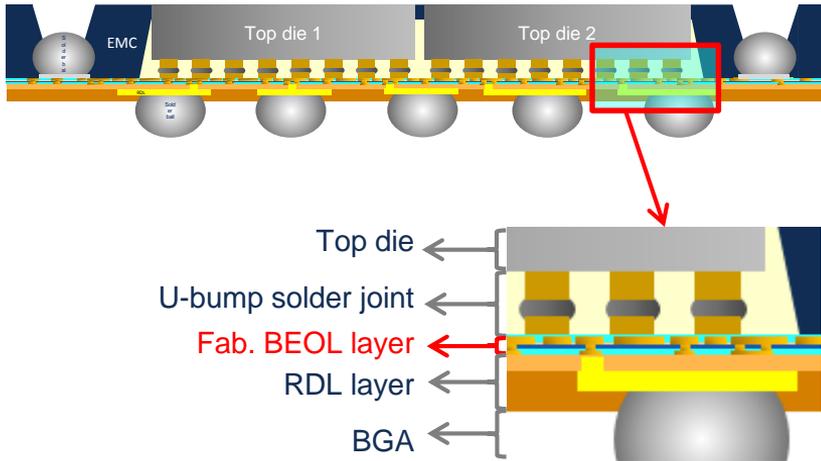
Amkor's Package Technology Integration Roadmap



SLIM & SWIFT Package Definition

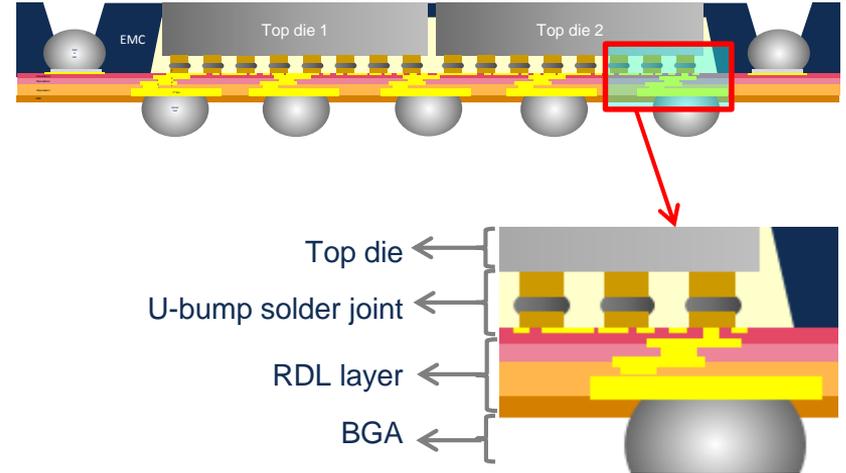
SLIM™

Silicon-Less Integrated Module

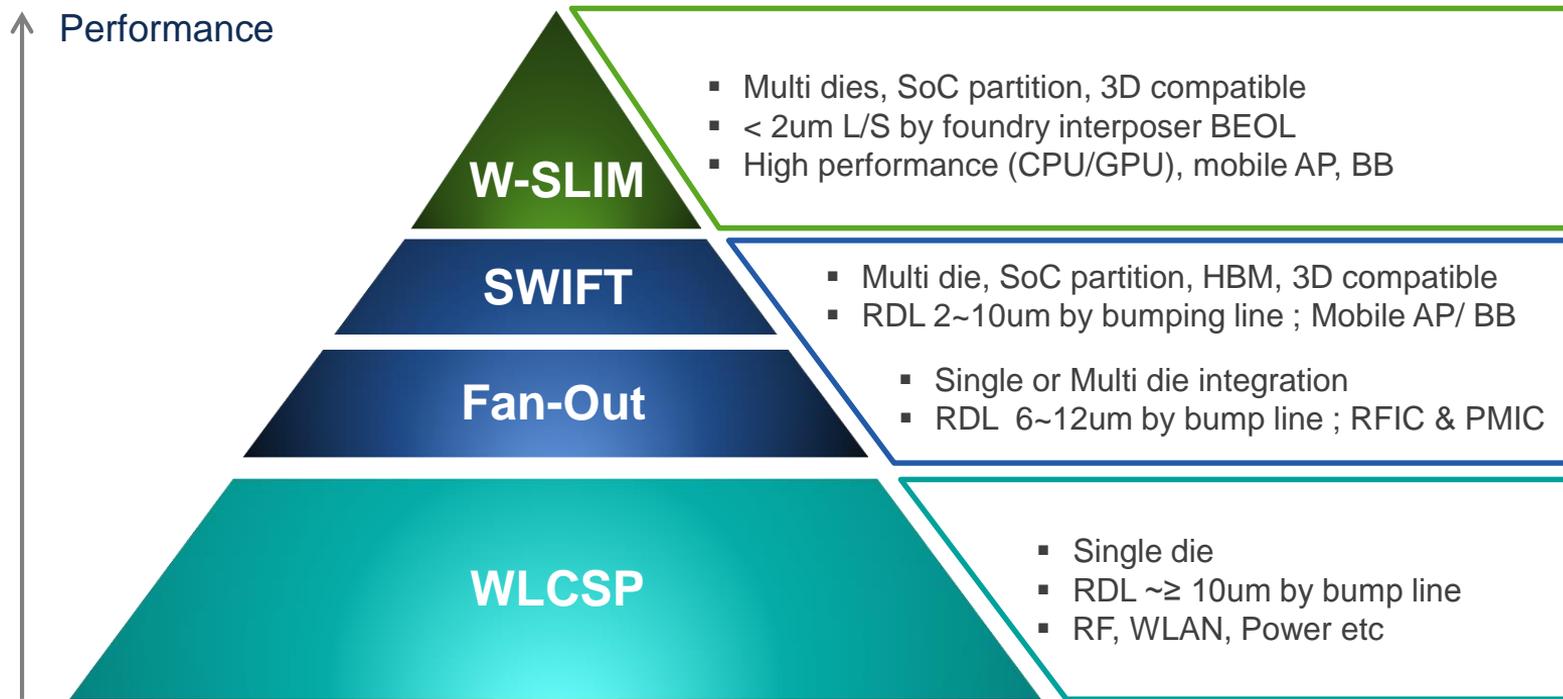


SWIFT™

Silicon Wafer Integrated Fan-out Technology

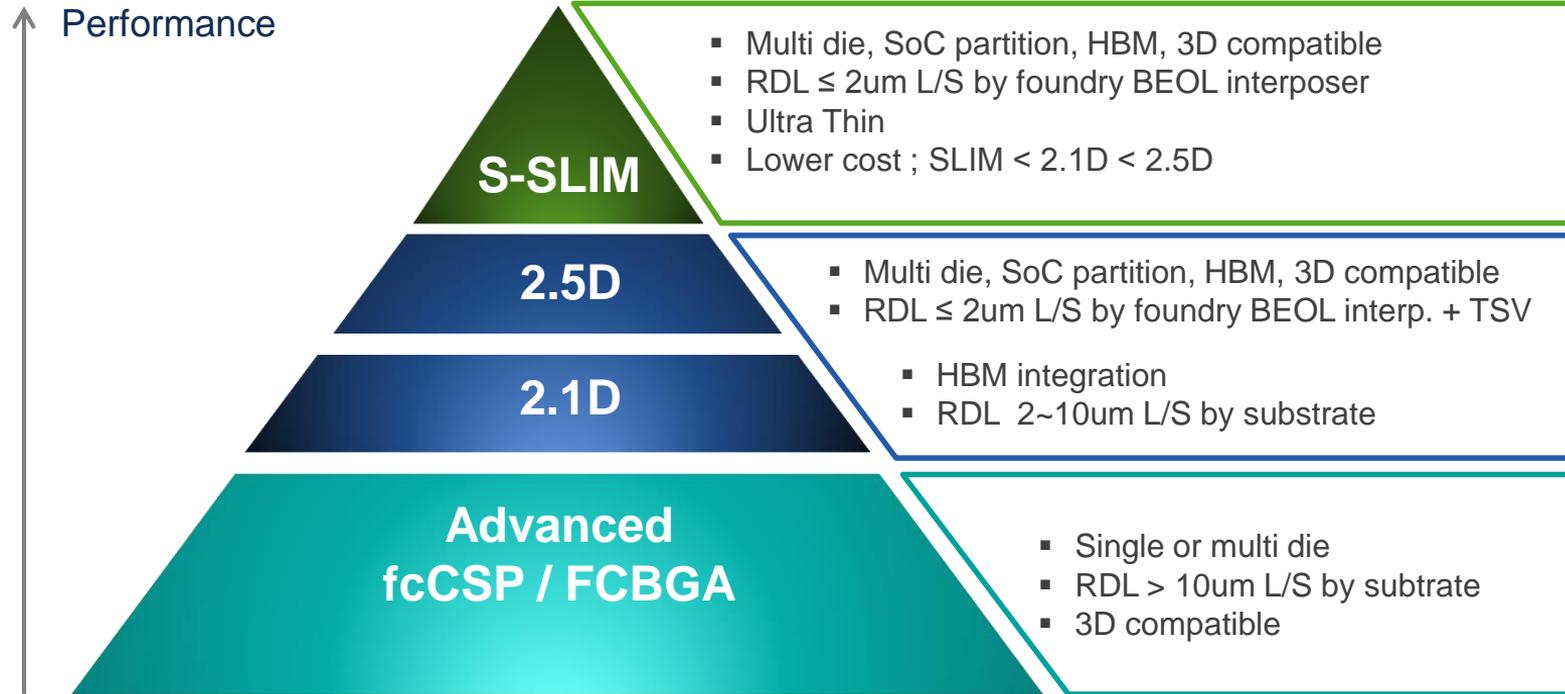


Amkor's Advanced Wafer Product Positioning



Products : RF and Analog to Advanced Processors

Amkor's Advanced Flip Chip Product Positioning



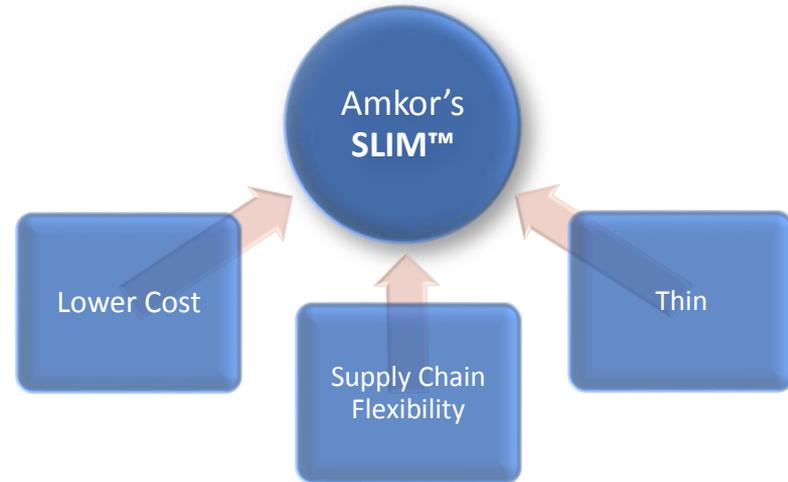
Products : AP, BB, CPU, GPU and Networking

SLIM Platform Technology

Amkor's Advanced Flip Chip Package Platform

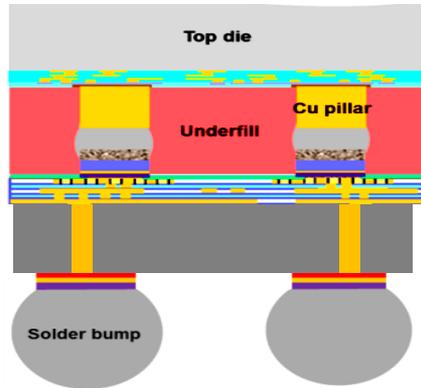
SLIM™: Value Proposition

- **Lower Cost**
 - Simplified wafer construction
 - Simplified wafer processing
- **Supply Chain Flexibility**
 - No longer tied to TSV formation
- **Reduction in Package Thickness**
 - Simplified wafer construction
 - Elimination of wafer back-side process steps compared to 2.5D
- **Leverages 2.5D wafer processing and assembly equipment and expertise**



SLIM™: Amkor's Most Advanced Packaging Solution

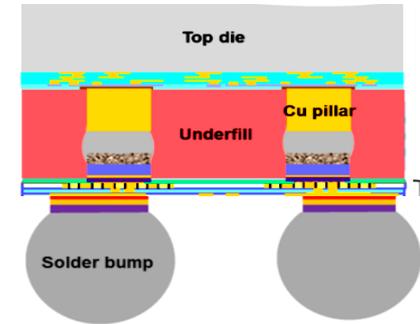
Silicon-Less Integrated Module (SLIM)



2.5D TSV
Si Interposer

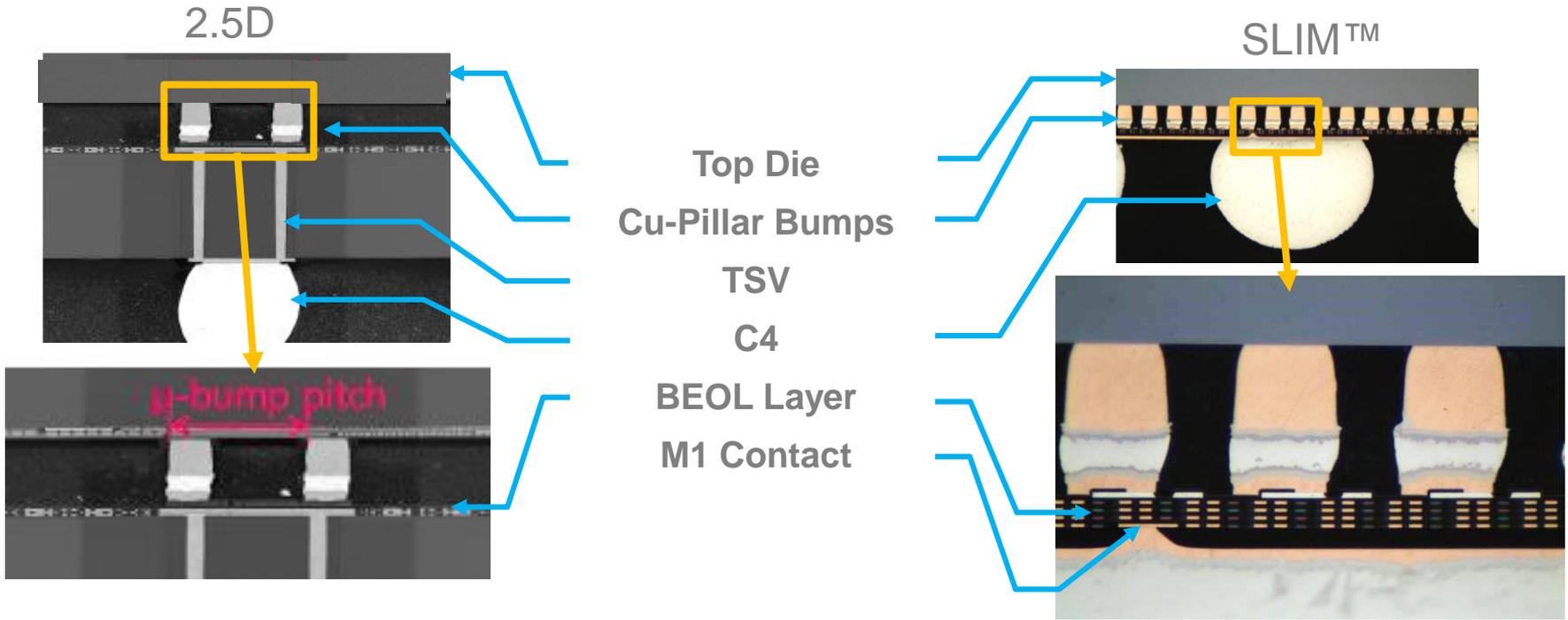


- Foundry BEOL layers retained
- Same CuP bond pads
- Same UBM and solder bump
- No TSV
- Much thinner

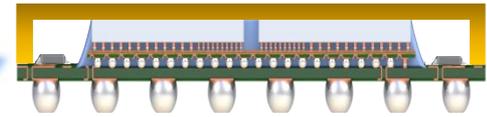
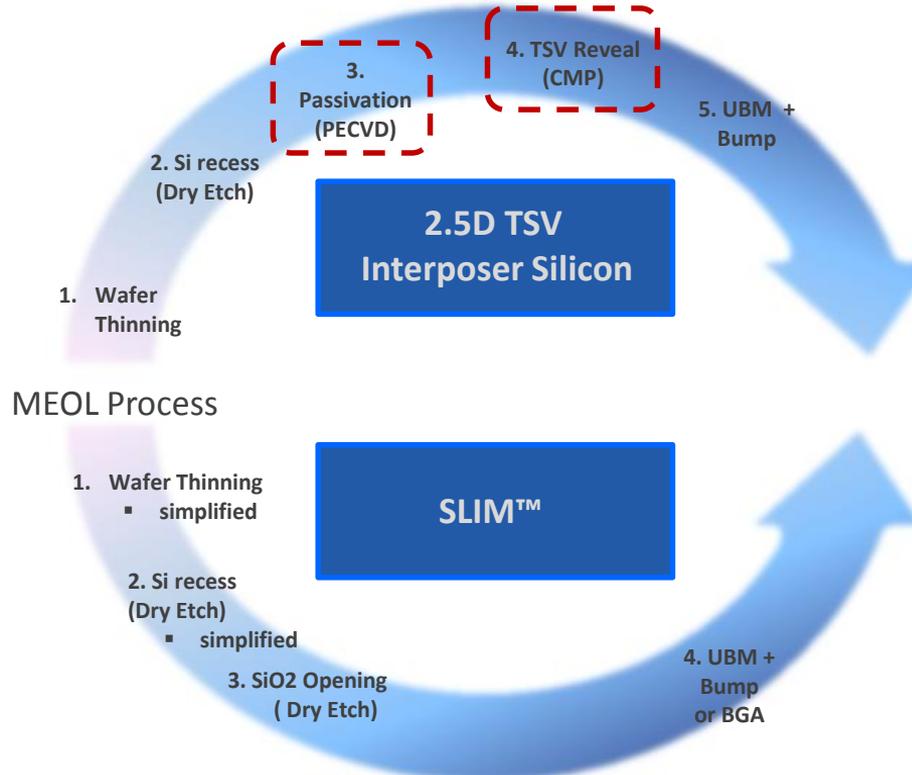
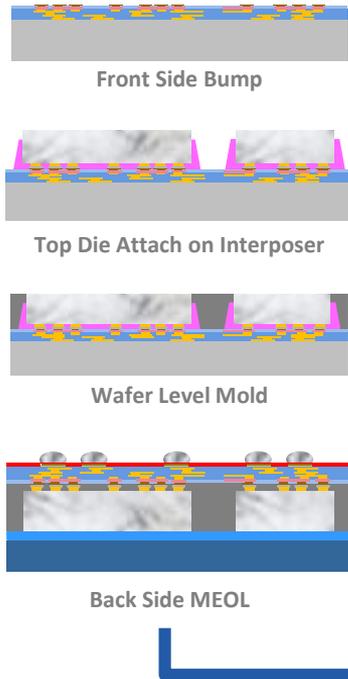


SLIM™
(non-TSV interposer)

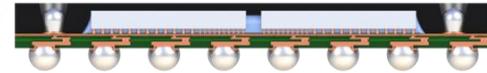
SLIM™ // 2.5D Construction Comparison



SLIM: Process Simplification

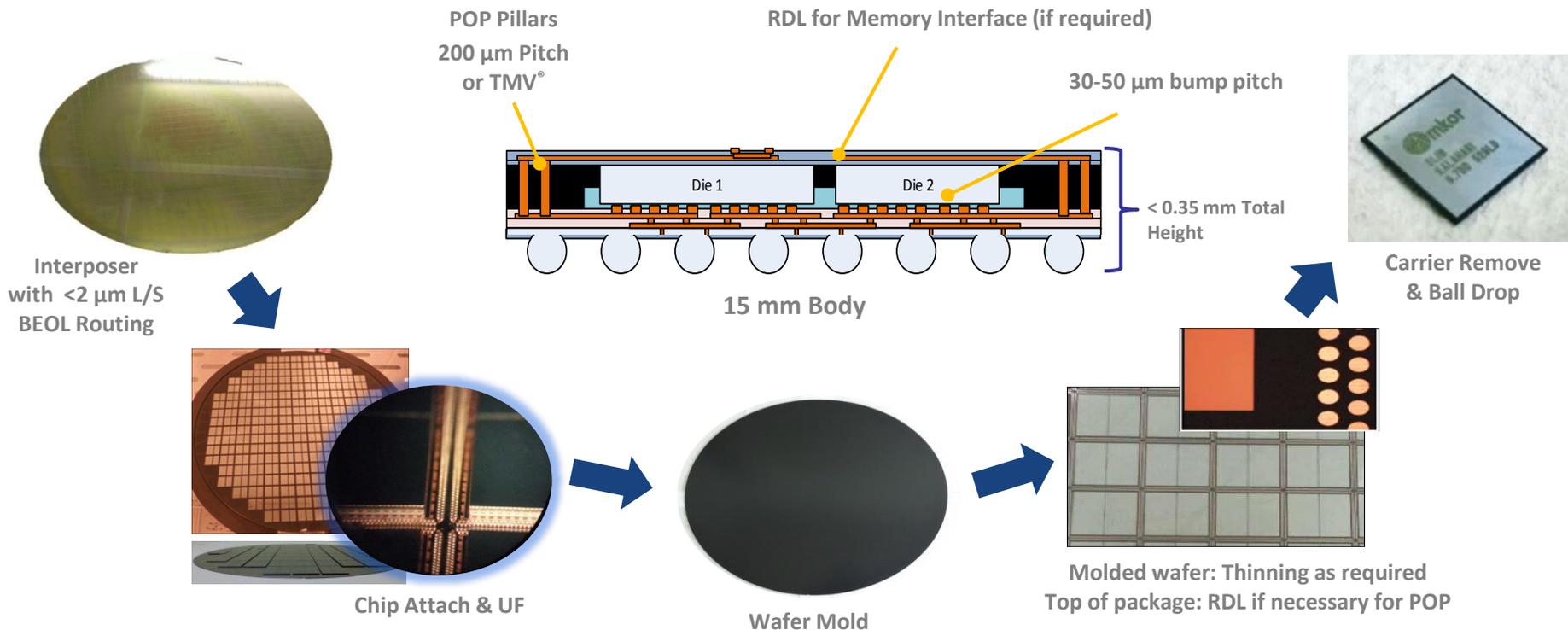


2.5D TSV

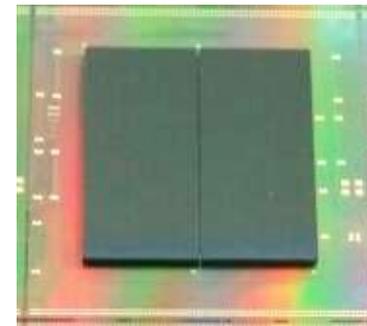
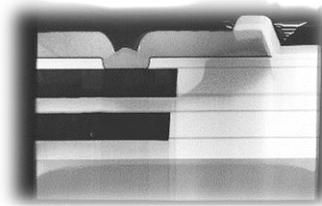


Wafer-level SLIM™ 2 Die 3D

SLIM™ Package Assembly Flow

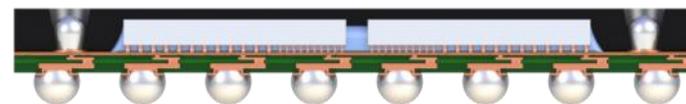


SLIM™ Test Vehicle – TV1

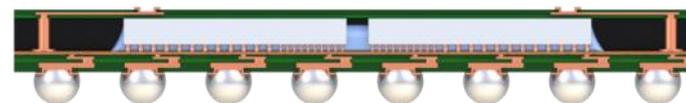


- Package size: 15 mm x 15 mm
- Top die:
 - Two die, sizes: 5 mm x 10 mm
 - 30 μm pitch minimum
- Flexible TMV® pad pitch
 - 150-400 μm
- Foundry BEOL
 - 2 Cu, 1-Aluminum, 1=RDL backside
- Die information
 - Top die bump count: 4800 (per die)
 - Die to die spacing: 100 μm
- Electrical Characterization
 - Impedance and cross talk

▪ Package structure



SLIM™ 2 Die Overmold

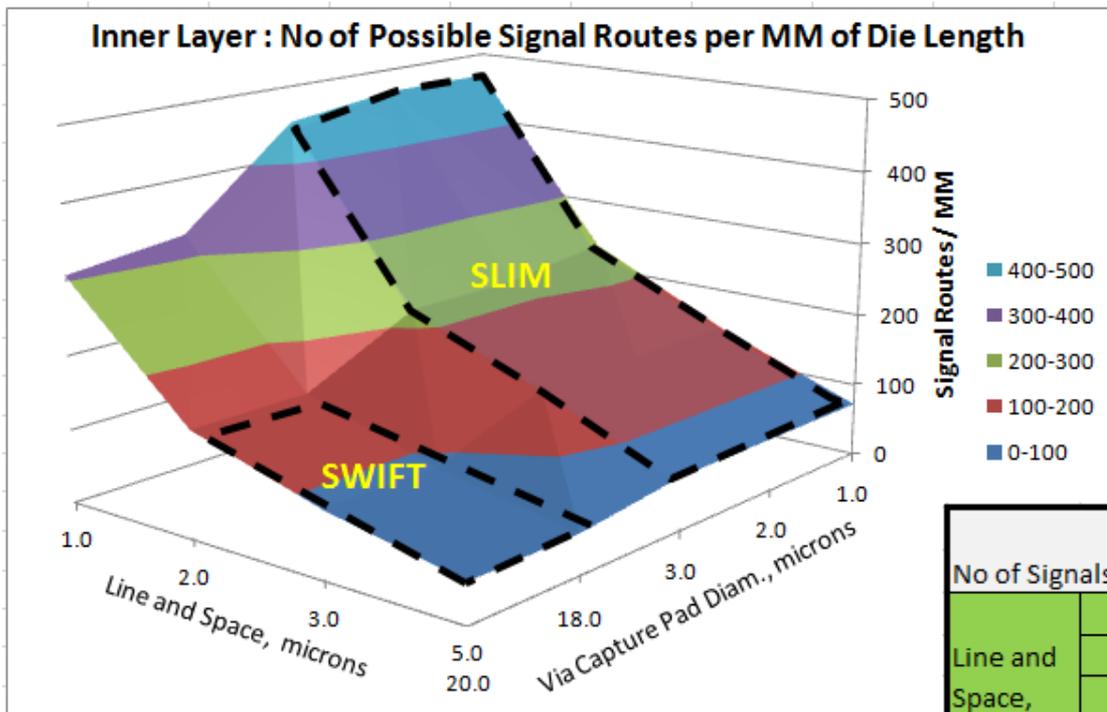


SLIM™ 2 Die Fan-in PoP

▪ Status

- On-going package rel builds
- One month staggered
 - CLR and BLR

SLIM vs SWIFT Signal Routing Capacity



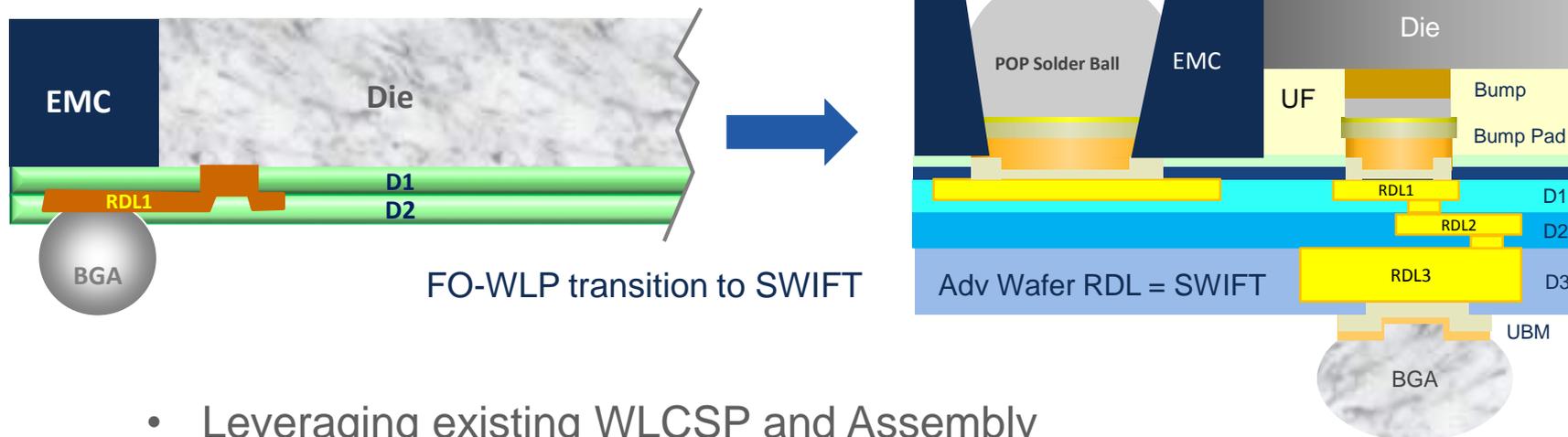
No of Signals/MM		Via Capture Pad Diameter, microns				
		1.0	2.0	3.0	18.0	20.0
Line and Space, microns	1.0	468	468	450	324	306
	2.0	234	216	216	144	144
	3.0	144	144	144	90	90
	5.0	72	72	72	54	54

SWIFT Platform Technology

Amkor's Advanced Wafer Fan-Out Platform

SWIFT: Amkor's Advanced Fan-Out Package

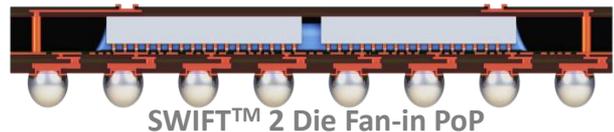
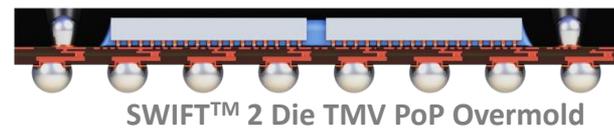
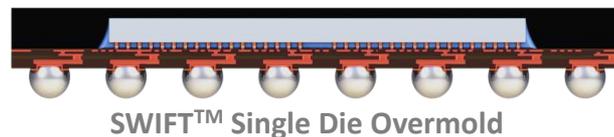
- SWIFT™ : Silicon Wafer Fan-Out Technology



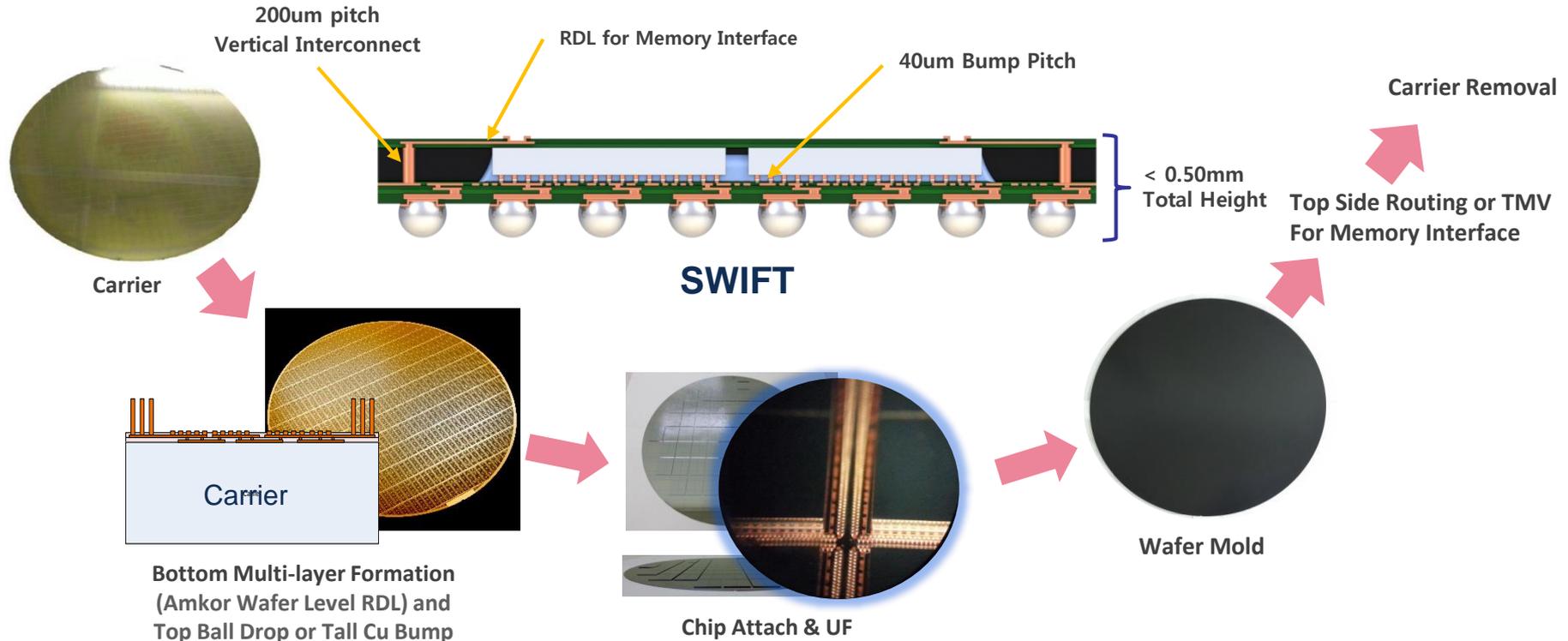
- Leveraging existing WLCSP and Assembly infrastructure and materials

SWIFT Value Proposition

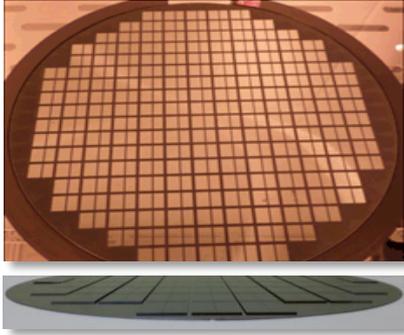
- Target Markets
 - Mobile, Networking
 - BB, AP, Logic + Memory, Deconstructed SoC
- Utilizes Existing Bump and Assembly Capability
 - Polymer based
 - Flexible
 - Multi-die and large die capability
 - Large package body capability
 - Advanced die integration
 - Stepper capability down to 2um line/space
 - Die shift / orthogonal rotation elimination
 - Down to 30um in-line copper pillar pitch
 - 3D capability
 - Package stack capability using Cu pillars or TMV



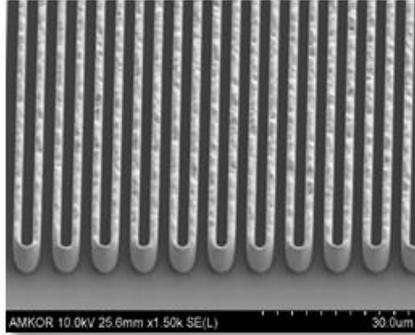
Silicon Wafer Integrated Fan-out Technology



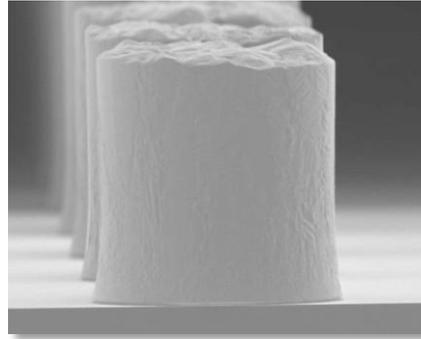
SWIFT Key Enabling Process Technologies



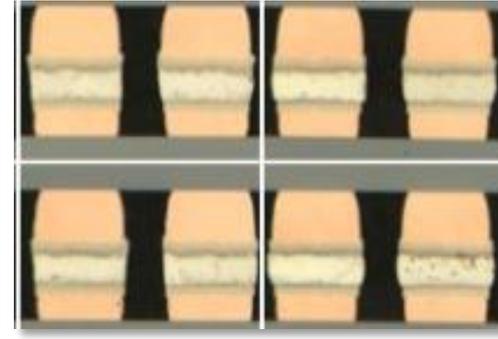
300mm with mold capability



Fine L/S RDL $\geq 2\mu\text{m}$
Stepper capability
Multilayer to 3 layers



Through mold interface
(Tall Cu Pillar or TMV)
 $> 100\mu\text{m}$ tall CuP bump



Fine pitch u-bump interconnection
40um pitch qualified
30um pitch demonstrated

Thank You!

Ron.Huemoeller@amkor.com