OPTICAL TECHNOLOGIES FOR TSV INSPECTION

Arun A. Aiyer,
Frontier Semiconductor
2127 Ringwood Ave, San Jose, California 95131

ABSTRACT:
In this paper, Frontier Semiconductor will introduce a new technology that is referred to as Virtual Interface Technology (VIT™). VIT™ is a Fourier domain technique that utilizes temporal phase shear of the measurement beam. The unique configuration of the sensor enables measurement of wafer and bonded stack thicknesses ranging from a few microns to millimeters with measurement repeatability ~ nm and resolution of approximately 0.1% of nominal thickness or depth. We will present data on high aspect ratio via measurements (depth, top critical dimension, bottom critical dimension, via bottom profile and side wall angle), data on debris inspection at via bottom, bonded wafer stack thickness, and Cu bump measurements. A complimentary tool developed at FSM is a high resolution μRaman spectrometer to measure stress-change in Si lattice induced by TSV processes. These measurements are important to determine Keep-Out-Zone in the areas where devices are built so that the engineered gate strain is not altered by TSV processing induced strain. Applications include via post-etch; via post fill, and bottom Cu nail stress measurements. The capabilities of and measurement results from both tools are discussed below.

KEY WORDS:
Virtual Interface Technology, TSV, Bottom CD, Profile, μRaman, Keep-out-zone

INTRODUCTION:
In the realm of 2.5D/3D packaging, a high throughput/production ready metrology tool with a single high-performance sensor that addresses multiple measurement-needs throughout the process flow, from FEOL to BEOL, can be very valuable in terms of yield improvement, cost of ownership reduction and tools utilization. A metrology tool developed at FSM based on Virtual Interface Technology (VIT™) has demonstrated its ability to be useful in the front end where the measurement features are only a few μm thick/deep and in the backend where the measurement range spans out to be several millimeters. Thus this technology can provide tool to tool compatibility at different measurement infliction points along a process line. High resolution μRaman can profile lattice stress around filled TSVs

DISCUSSION:
VIT™ is a Fourier domain technique that utilizes temporal phase shear of the measurement beam. The unique sensor configuration enables creation of non-physical interfaces which enhance tool measurement capabilities in terms of measurement range, accuracy and repeatability. One example of how this technology is used in thick substrate measurement is demonstrated with help of figures 1, 2 and 3. Illumination can be from front side or backside of the sample.

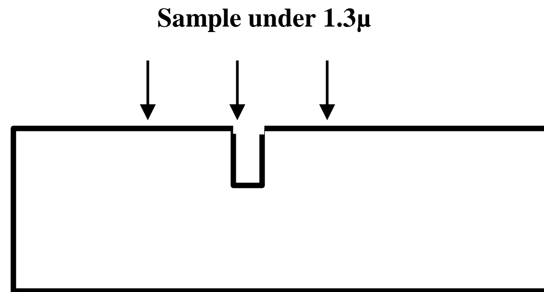

Figure 1. Schematic of TSV sample under illumination

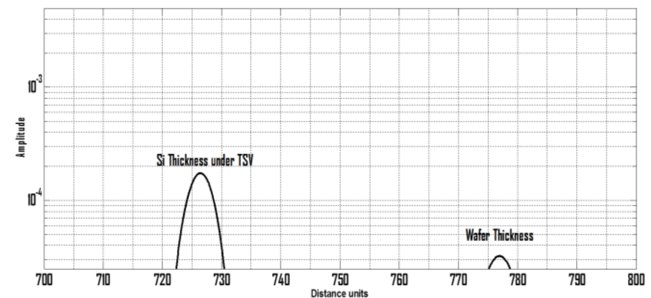

Figure 2. Thickness spectrum without enabling VIT™

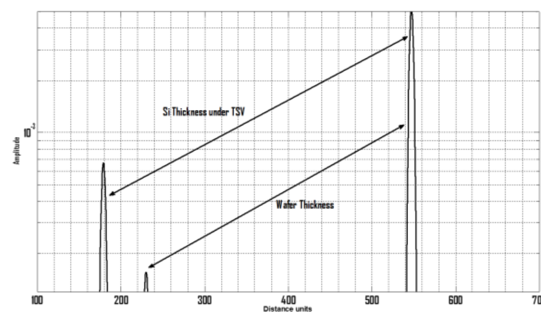

Figure 3. Thickness spectrum with VIT™ enabled

An examination of signal amplitudes in figures 2 and 3 immediately reveals the effectiveness of VIT™ in thickness measurement. When VIT™ is enabled, the signal pairs used in determining wafer thickness and thickness under the TSV are 5x or more strong than the signal amplitudes without VIT™. Stronger signals improve measurement accuracy and repeatability. Thickness of a 300mm wafer mapped using this approach is shown in figure 4. The 1σ standard deviation achievable by this technique is given in In Table 1.

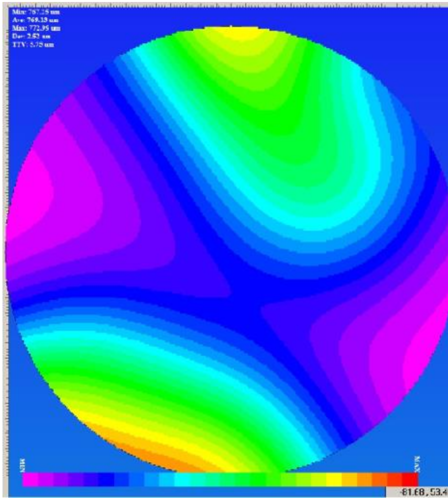

Figure 4. Thickness map of a 300mm wafer. TTV 5.75µm

Table 1. Thickness Measurement Repeatability

Repeats	Wafer Thickness µm
1	772.837
2	772.841
3	772.841
4	772.841
5	772.837
6	772.837
7	772.837
8	772.841
9	772.837
10	772.837
Average	772.838
1σ Static Repeatability	0.0018

The 1σ static repeatability is < 2nm while the nominal 1σ w/o VIT™ is ≥100nm.

Measuring TSV Parameters with VIT™

The parameters to be measured are shown in figure 5.

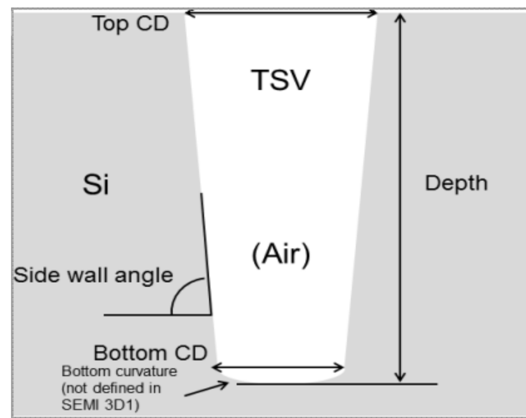

Figure 5. TSV schematic showing parameters to be measured[1]

Depth: The VIT™ enabled thickness spectrum is displayed in figure 6. This spectral signature is typical from a sample like that shown in figure 1. Peaks A, B, C, D and E appear

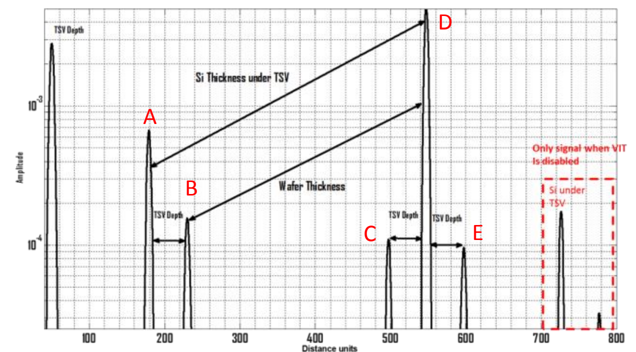

Figure 6. VIT™ enabled thickness spectrum that facilitates simultaneous measurement of thickness, depth & via profile

only when VIT™ is enabled. It is important to note that the separation between peaks A/B, C/D, and D/E is same as the TSV depth value which is independently given by the first peak in the spectrum. Thus VIT™ has a self-checking mechanism built into it when measuring via depth.

Table 2. Depth and static repeatability of 5x50 μm^2 TSV

Repeats	Depth in µm Average of 10 measurements	1σ Repeatability µm
1	49.629	$\sim 10^{-3}$
2	49.626	$\sim 10^{-3}$
3	49.629	$\sim 10^{-3}$
4	49.630	$\sim 10^{-3}$
5	49.629	$\sim 10^{-3}$

Table 3. Depth & dynamic repeatability of 12x100 μm² TSV

Repeats	Depth μm
1	100.40
2	100.24
3	100.43
4	100.13
5	100.49
6	100.52
7	100.44
8	100.33
9	100.52
10	100.12
Average	100.367
Semi Dynamic 1σ Repeatability	0.15

Map of depth variation in a sample with 5x50 μm² vias is given in figure 7.

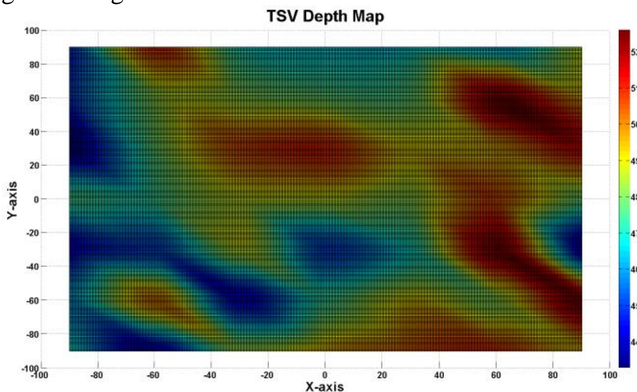

Figure 7. TSV depth map. Total depth variation = 9μm.

TSV bottom CD: Peak D in figure 6 results from virtual interfaces while peaks C and E are from the coherent interaction of virtual interface with the interface defined by via bottom. TSV "optical" bottom CD (BCD) is calculated using area under these peaks. Thus this is not a model based approach. Table 4 compares the computed BCD with that measured with an IR camera which has a pixel resolution of 0.3μm/pixel. TCD in the table refers to via diameter measured with the same IR camera. Knowing top and bottom CDs, the sidewall angle (SWA) is determined. Similar measurements taken with the 12x100 μm² via sample are given in Table 5. From these two data sets one can see that the 100μm deep via is tapered more near the bottom.

VIT™ can be engineered to measure TSV parameters either from wafer front side and/or backside. So a bottom probe may be used for profile measurement even if the via is filled.

Bottom **P**rofile in **R**eveal **CMP**: For Cu nail reveal process it is important to know the via bottom profile, since it is required to polish far enough into the TSV to remove rounded profile at the via base. This is shown schematically in figure 8[2]. In reveal CMP the time required from Cu tip exposure to complete via reveal can be several minutes and *a priori* knowledge of parameter "b" can be valuable in controlling the CMP process. We have demonstrated VIT™'s ability to measure bottom profile and the "b" parameter and the result of one such measurement is shown in figure 9.

Table 4. Bottom CD and Side Wall Angle of 5x50 μm² vias

Repeats	BCD with VIT™ μm	BCD (from backside) with IR Camera μm	SWA deg.
1	3.63	3.3	89.49
2	3.66	3.3	89.50
3	3.70	3.6	89.51
4	3.66	3.6	89.50
5	3.57	3.3	89.47
Average	3.65	3.42	89.49
Static 1σ	0.051		0.014

Table 5. Bottom CD and SWA of 12x100 μm² vias

	TCD	11.8 μm
Repeats	**BCD μm**	**SWA deg.**
1	8.69	89.11
2	8.61	89.09
4	8.67	89.10
5	8.64	89.09
6	8.58	89.08
7	8.64	89.09
8	8.70	89.11
9	8.64	89.10
10	8.70	89.11
11	8.63	89.09
12	8.66	89.10
13	8.78	89.14
14	8.78	89.14
Average	8.67	89.11
Static 1σ	0.059	0.017

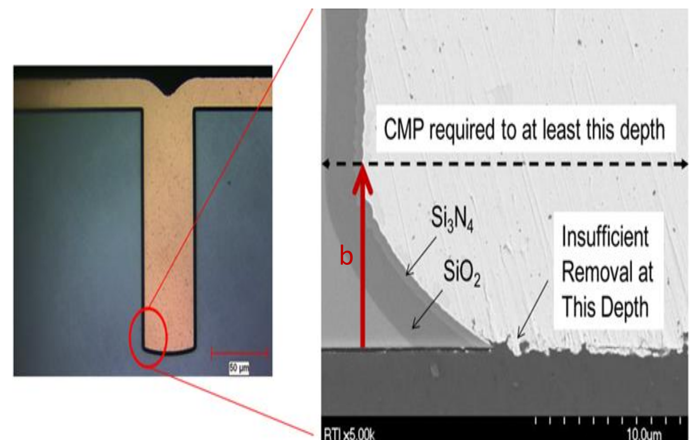

Figure 8. Bottom Profile for TSV Reveal. Source: Entrepix

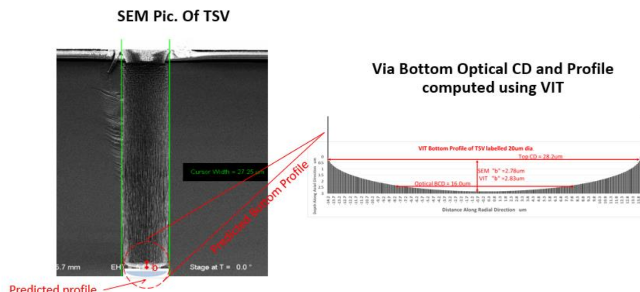

Figure 9. TSV bottom profile: "b_{SEM}"=2.78µ, "b_{VIT}"=2.83µ

In calculating the "b" parameter it is assumed that the bottom profile can be represented by a prolate ellipsoid with the TSV diameter as its major axis and "b" as its semi-minor axis.

C4 and **M**icro **B**ump **M**easurement: C4 and µBump arrays can be measured with VIT^{TM}. The height maps of these measurements are given in figures10 and 11

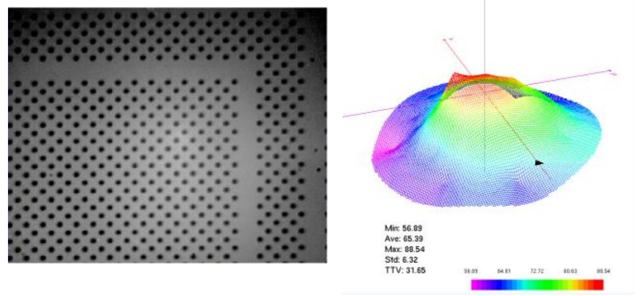

Figure 10. C4 Bumps on an 88µm thick wafer

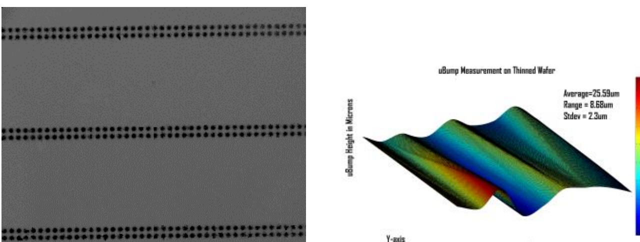

Figure 11. µBump Height Map on a 90µm thick wafer

Mapping **H**ighly **W**arped **BWS**:
A warped bonded wafer stack comprising of carrier wafer, Si layer and embedding compound has been mapped for individual thickness

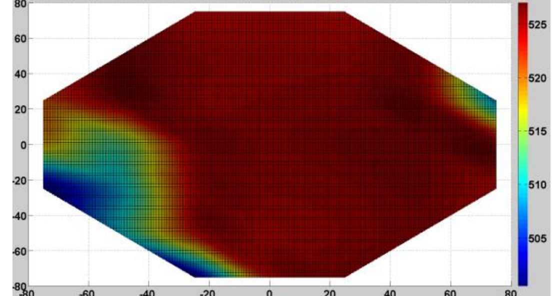

Figure 12a. Carrier wafer thickness map. TTV=25.87µm

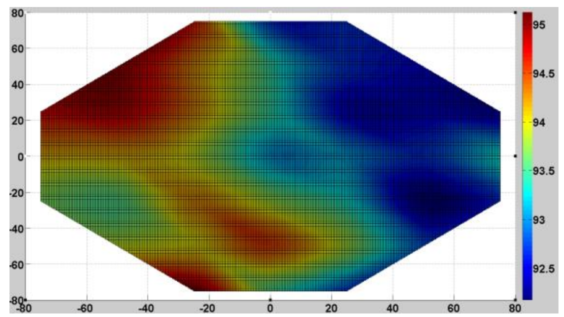

Figure 12b. Si wafer thickness map. TTV=2.93µm

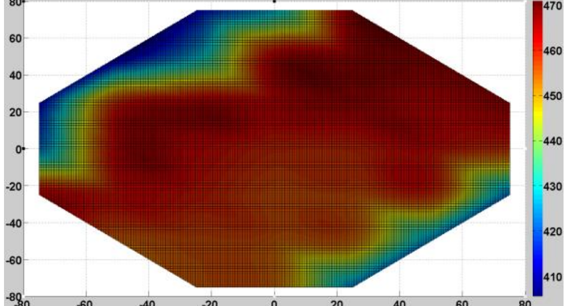

Figure 12c. Layer thickness map. TTV=60.76µm

Measuring **T**hickness of **T**hinned **W**afers: Figure 13 shows the image of the device side of a BSI-CIS wafer from the thinned Si side. VIT^{TM} has demonstrated its ability to measure such highly thinned Si wafers as well. Thicknesses measured on seven such samples are tabulated in Table 6.

Table6. BSI-CIS Wafer Thickness

	Thickness µm	1σ St.Dev. µm
Wfr8	4.35	0.058
Wfr12	3.32	0.051
Wfr 13	3.96	0.062
Wfr 14	3.36	0.064
Wfr 15	3.92	0.037
Wfr 24	4.09	0.064
Wfr 25	4.14	0.038

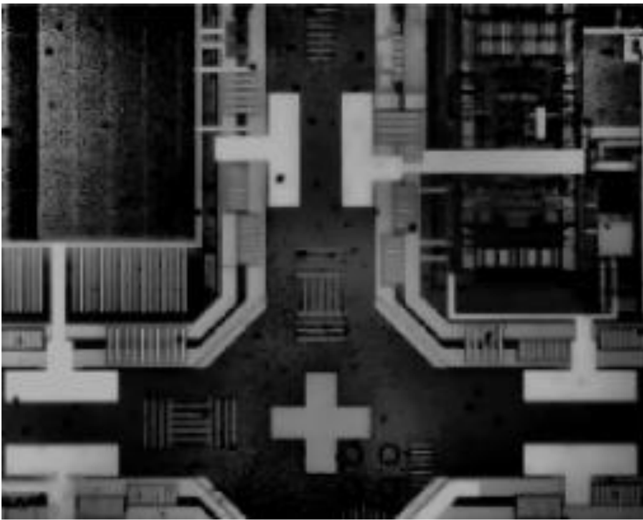

Figure 13. Device Image of BSICIS wafer from backside

μRaman for **TSV K**eep out **Z**one: A high resolution Raman spectrometer developed by FSM is capable of profiling stress change around a metal filled TSV before and after an anneal process. To measure stress profile, the Raman line in stressed sample is compared to that in unstressed Si. The shift between the two is used in calculating stress. This is schematically represented in figure 14.

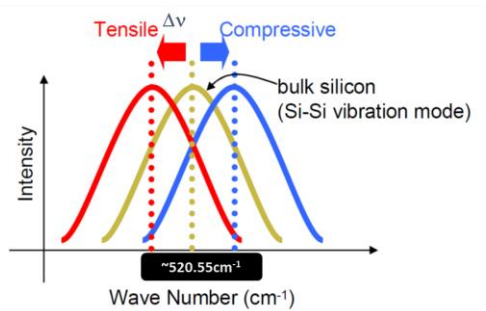

Figure 14. Relationship between stress and Raman spectra

From the peak shift, stress is calculated using the relationship Stress (MPa) = 475 x $\Delta\nu$ cm^{-1}.

Figure 15 shows part of metal filled TSV array that was used for measuring Keep-Out-Zone. Stress profile between two TSVs separated by 80 to 100μm has been measured. Figure 16 shows stress profile before and after anneal. The significant change in stress profile measured by Raman makes μRaman an indispensable process control tool in 3D-IC HVM. It must be mentioned here that these measurements were taken on two different samples where the pre-annealed sample has TSVs at 80μm pitch while that the post annealed sample has them at 100μm pitch. In figure 17 stress profile measured on several annealed samples with latter pitch is given.

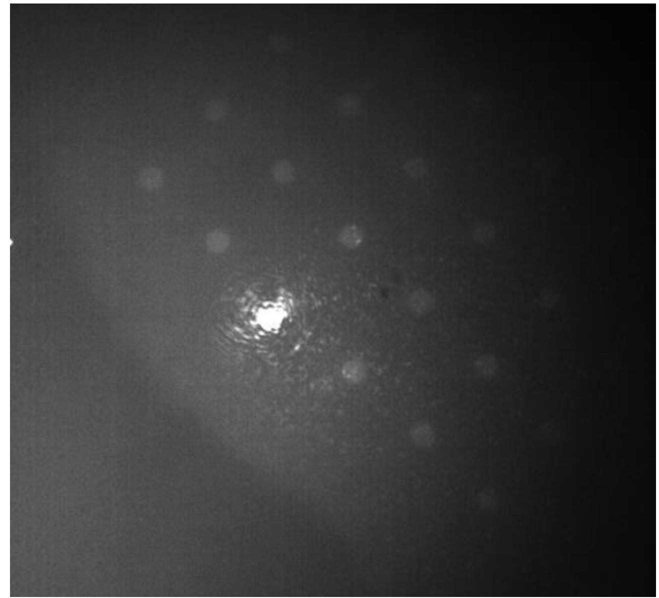

Figure 15. 5μm diameter filled TSVs with 100μm pitch

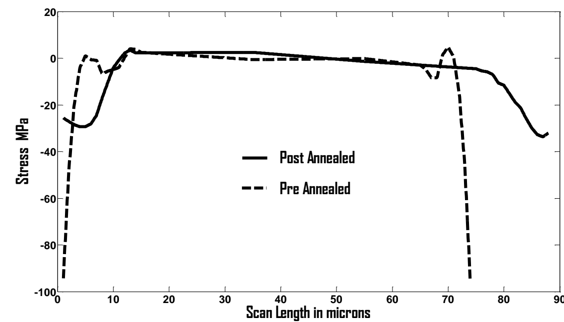

Figure 16. Stress profiles of pre-annealed and post-annealed TSV samples

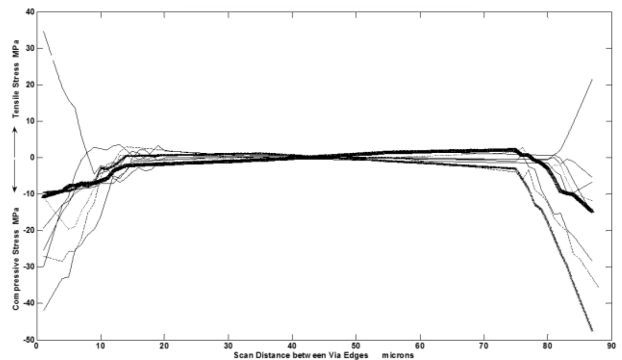

Figure 17. Stress profile of samples that have gone through different levels of anneal process

CONCLUSIONS:

The tool based on VIT^{TM} has a depth/thickness measurement range spanning a few microns to a few mms. This makes the tool capable of monitoring several FEOL and BEOL processes in 3D packaging applications. These iclude TSV depth and profile measurements; bonded wafer stacks measurement; thinned Si wafer measurement in RST and BSI-CIS applications; after reveal Cu nail co-planarity

measurement; and C4, μBumps & Cu pillar height measurements. The measurement repeatability shows that the tool is robust and is ideal for production environment. Such versatility enables flexible utilization of tools in production, provides full software compatibility, affords machine to machine matching. These factors in turn minimizes Operations & Service training and lessens spare parts inventory. Consequently tool downtime is reduced leading to better Cost of Ownership.

The μRaman tool has a spectral resolution of $0.05cm^{-1}$ and is therefore capable of measuring stress change as small as sub 25 MPa. Using this this tool we have demonstrated μRaman's ability to profile Keep-out-Zone in TSV enabled 3D packaging. Additionally, the significant reduction in stress values resulting from anneal process is readily mapped by this tool.

REFERENCES:

1. "SEMI Draft Document 5410- New Standard" Guide for Metrology Techniques to be Used in Measurement of Geometrical Parameters of TSV's in 3DS-IC Structures
2. "Overview of CMP for TSV's" presented at the NCCAVS Joint User Group Meeting by Rob Rhoads, Entrepix, June 11, 2013