



INNOVATION PUT TO THE TEST

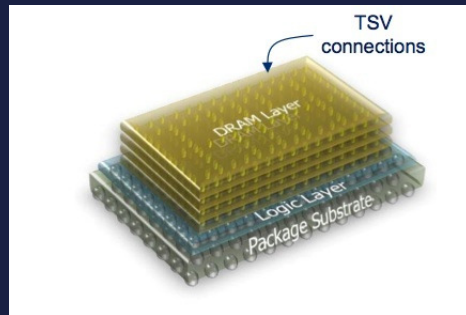


FORMFACTOR
Advanced Wafer Probe Solutions

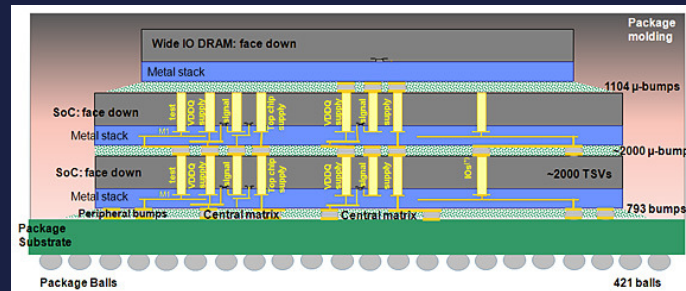
Direct Connection and Testing of TSV and
Microbump Devices using NanoPierce™
Contactors for 3D-IC Integration

- There is a paradigm shift in semiconductor industry towards 2.5D and 3D integration of heterogeneous parts to build complex systems.
- Similarly, industry needs a paradigm shift in testing also → a socketing test solution for bare die to enable KGD/KGS.

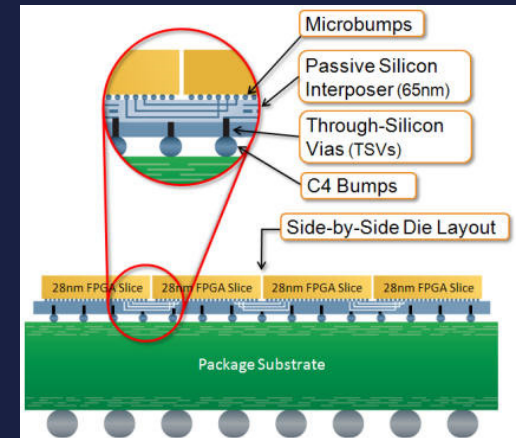
Motivation and future of TSV level integration



Hybrid Memory Cube
Micron, IBM, Samsung



Wide I/O 3D-IC logic and memory stack
CAE-LETI, ST-Ericsson, Cadence

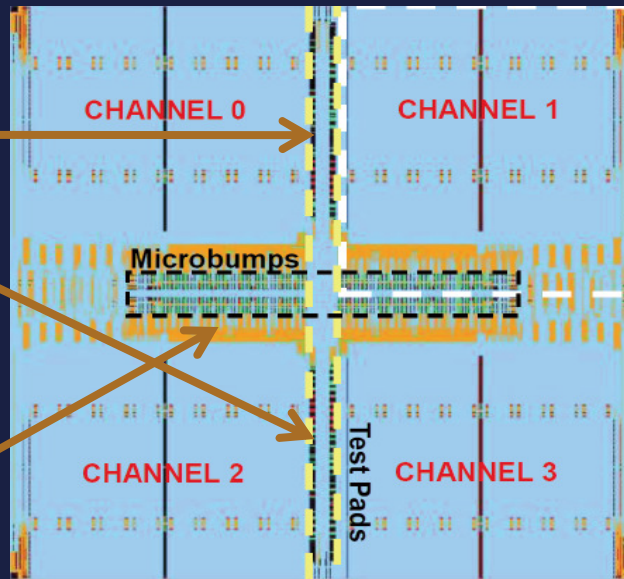


2.5D IC, Xilinx

- System assembly at the TSV level using heterogeneous devices from multiple suppliers is the goal
- Standard packages enable end system assemblers to build complex systems from multiple IC suppliers with confidence
- TSV devices must function like today's packaged parts in the system assembly flow
 - *Known Good Die at the TSV level*
 - *Known Good Stacks at the TSV level*

MicroBump/TSV Enabled Memory Die

Aluminum Pads - Available for Testing of Die Functionality (20-60 probed pads at High Parallelism)

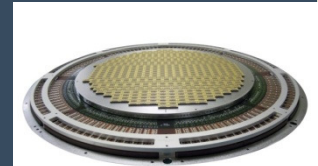


Source: ISSCC 2011 Samsung Electronics

MicroBump/TSV Region – potentially 1200 or more TSV interconnects per die

Current probe solutions for parallel memory test:

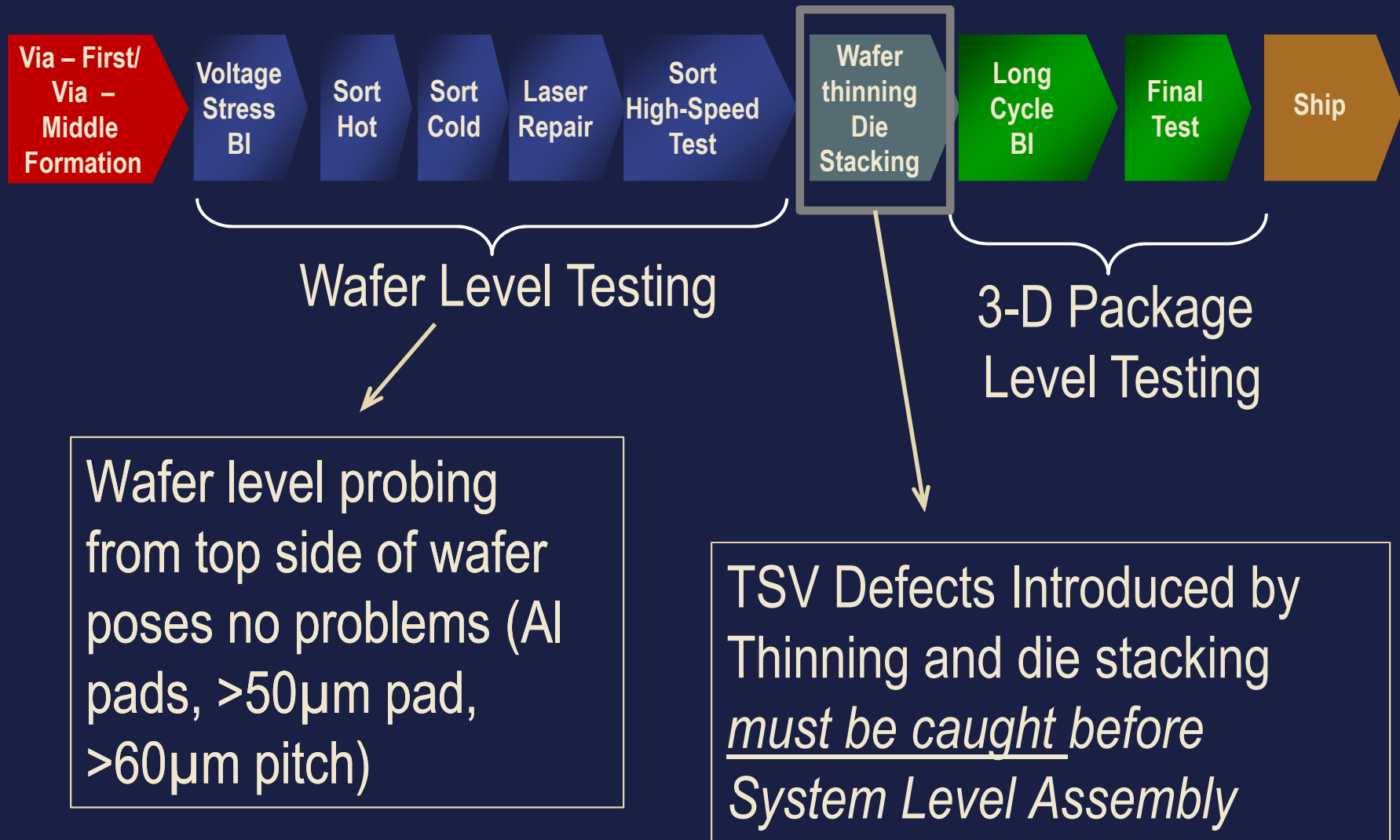
- 500-1000 DUT
- 20-60 pins per DUT
- 20K-60K Pins
- 50-200kgF



TSV interfaces with 1000's of pads/DUT will require 1000s of kgF prober force!

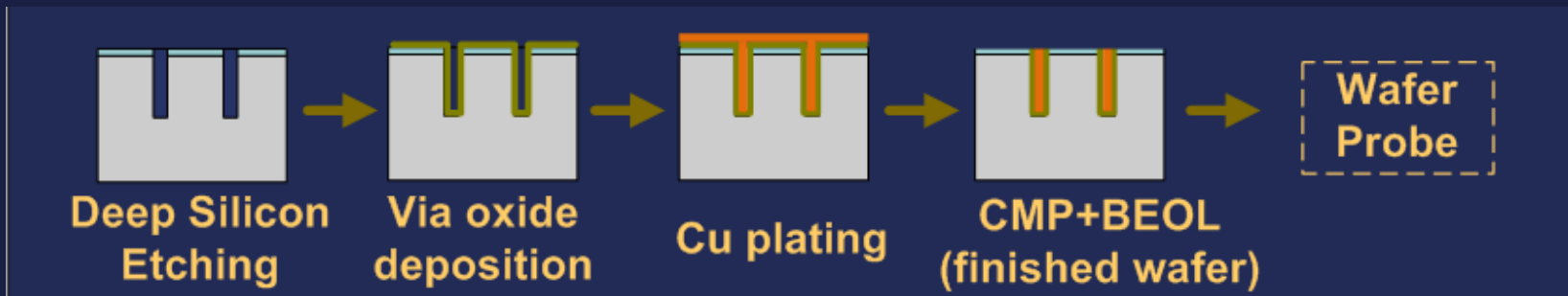
Very high signal counts that are the main benefit of TSV connection architectures make conventional wafer probing, particularly for memory devices which demand high parallelism, largely impractical.

DRAM TSV device test flow and the problem

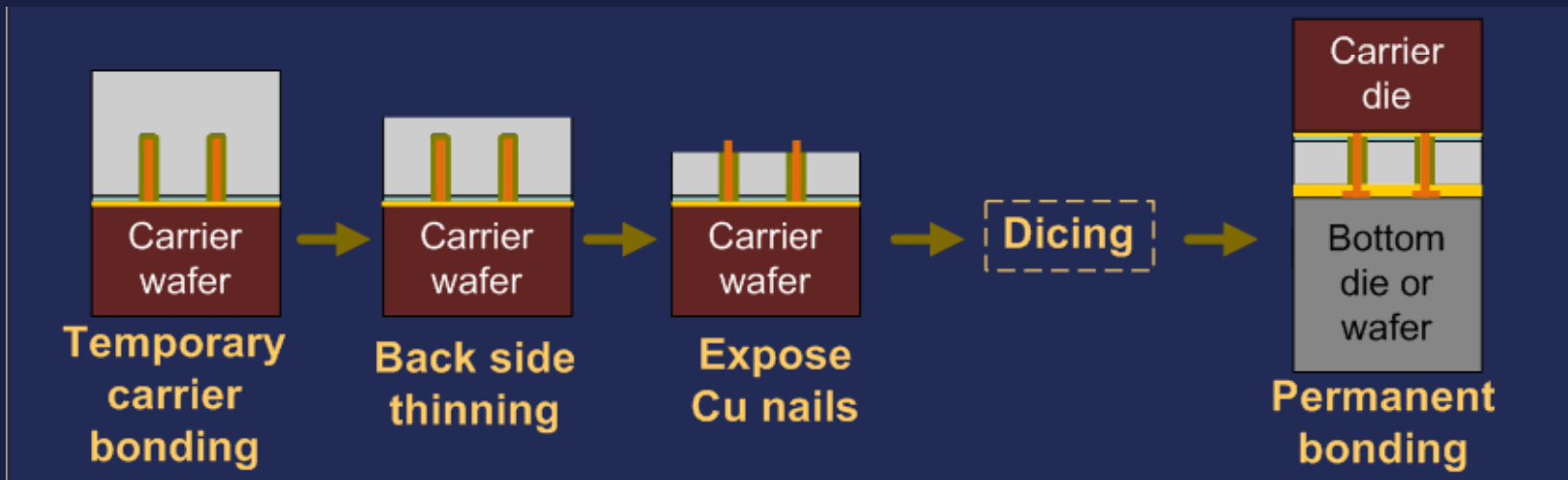


TSV Manufacturing Flow

TSV Formation



Wafer thinning and bonding

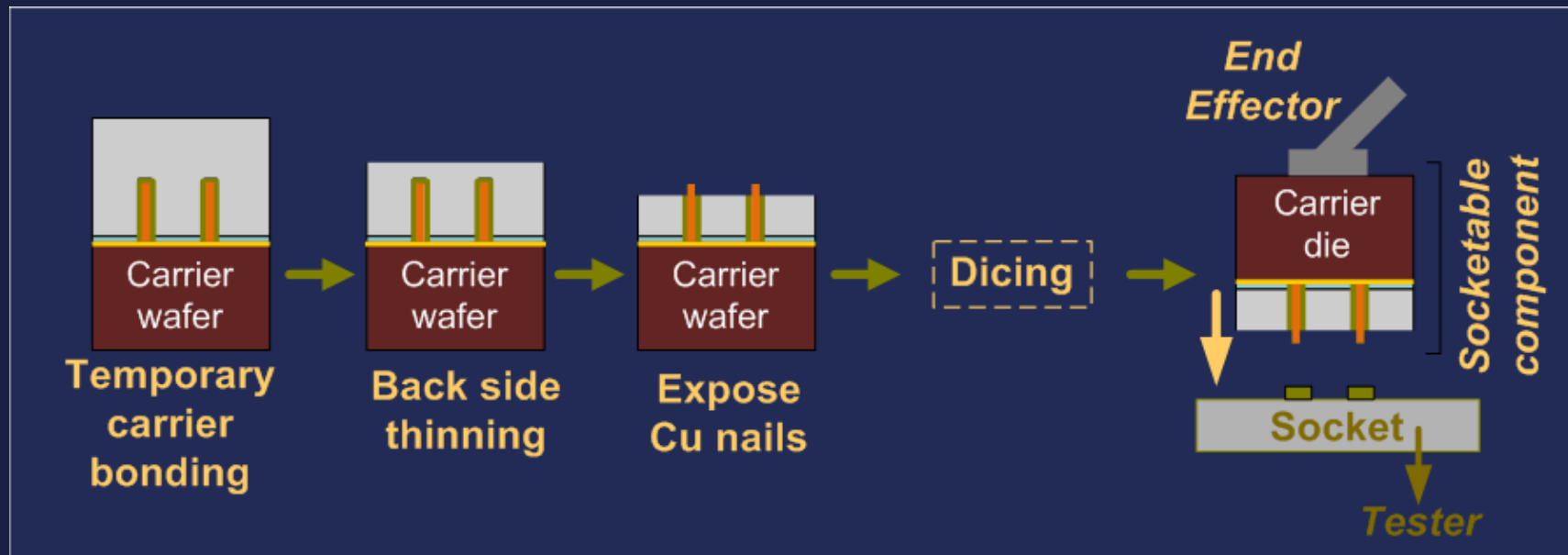


Source: E. J. Marinissen, Y. Zorian, Tutorial on Testing TSV-Based Three Dimensional Stacked IC's, ITC, Austin, TX, 2010

- Defects introduced by wafer thinning and dicing after the wafer probing step will not be detected.

Solution For KGD/ KGS of Thinned Die and stacks

Wafer Thinning and Socketing Prior to Bonding

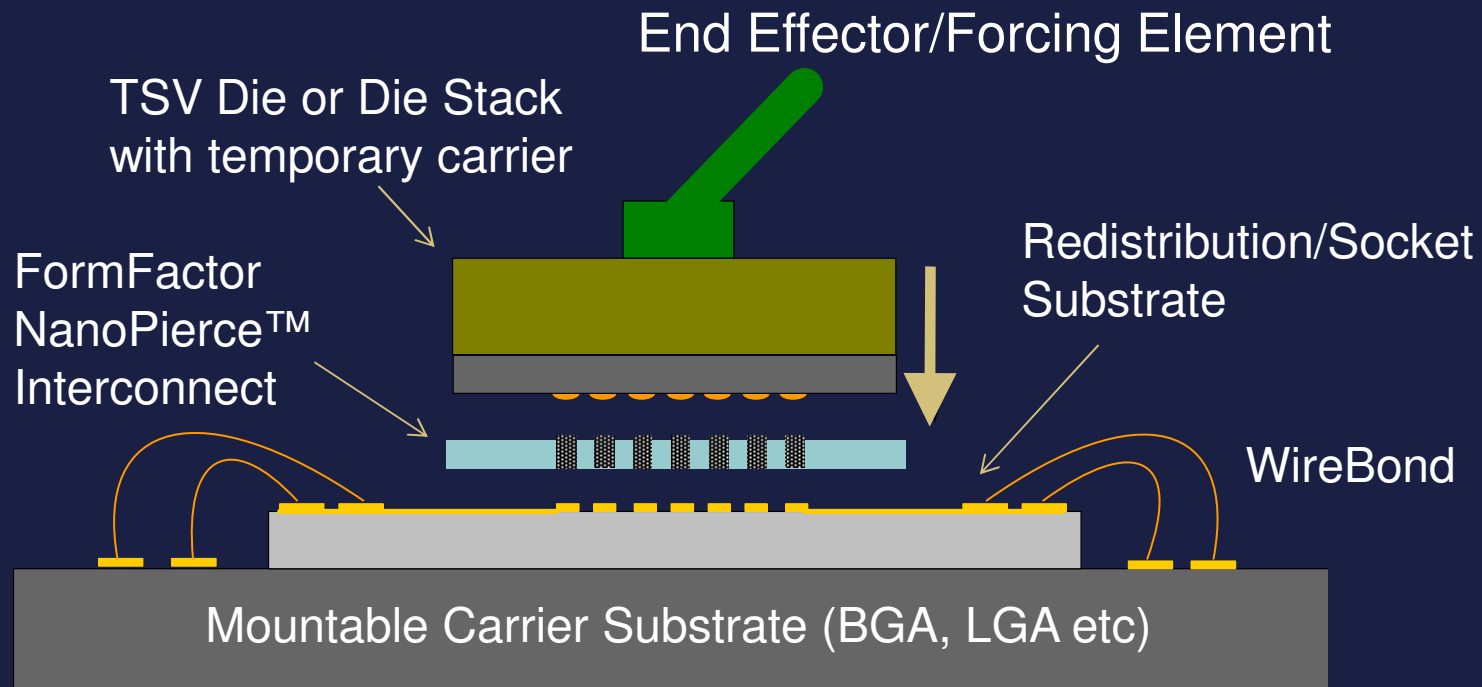


- Thinned die or stacks on carrier handles can be socketed for testing
 - Socket tested devices are then KGD/KGS for system assembly
- Similar to Today's Packaged Devices

Socket Solution Requirements for TSV Testing

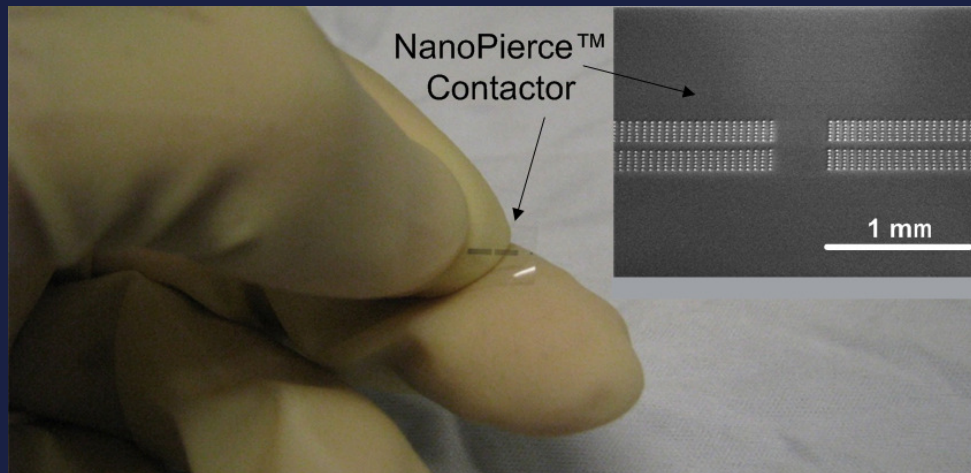
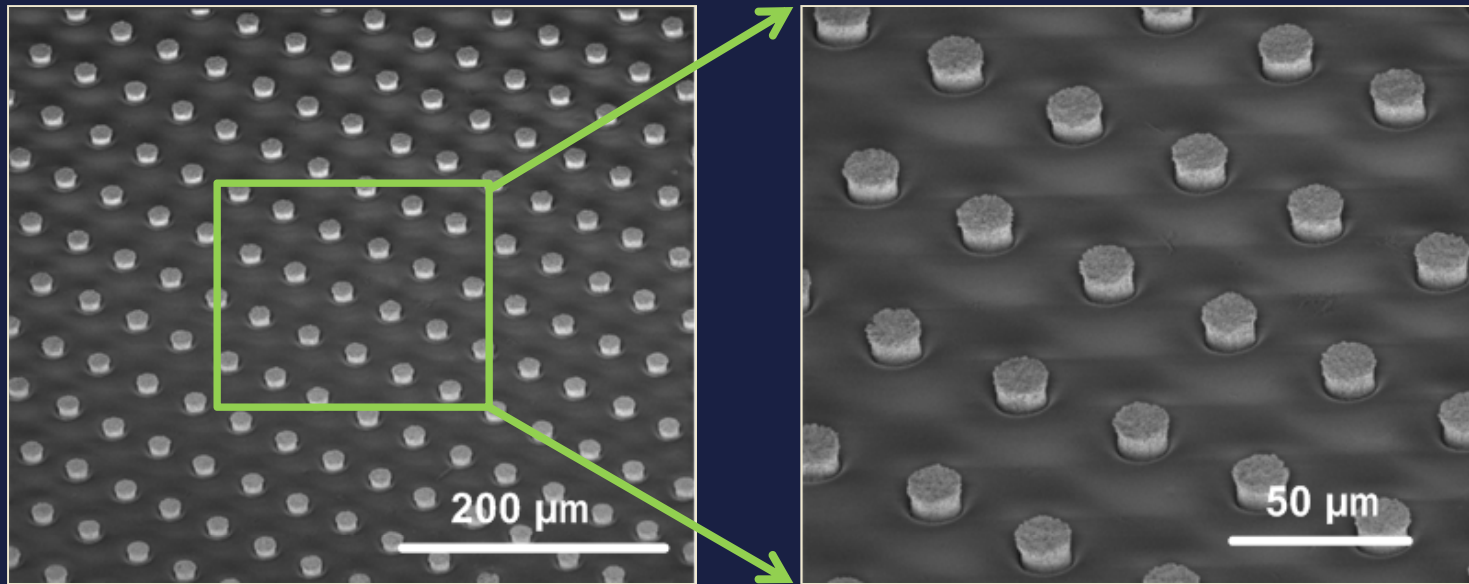
- Compliant contact interface at tight pitch
- Durable – 100,000s of Contact Cycles
- Scalable – Down to 20 micron array pitch or below
- Minimum damage – Socketing/testing cannot influence subsequent bonding steps
- Path Resistance – <10 Ohm/contact
- Low Inductance – If high frequency test required

Socketing of TSV Devices



- Forcing element can be robotic end effector or mechanical socket body
- Redistribution substrate does not require TSVs
- Standard TSV Interface Designs Enables Standard Sockets

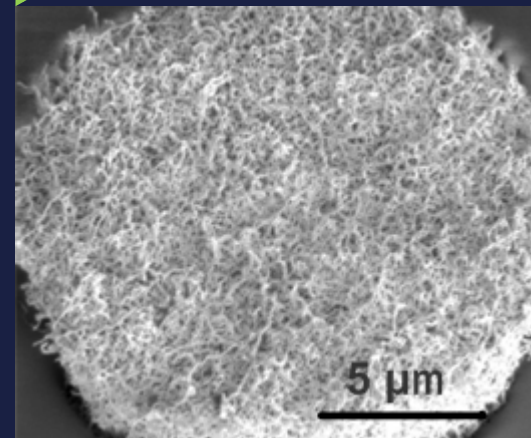
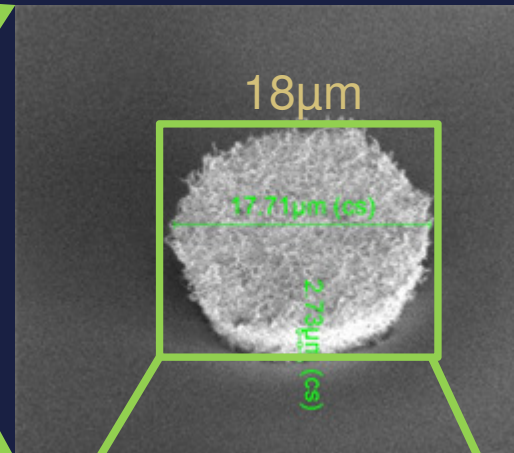
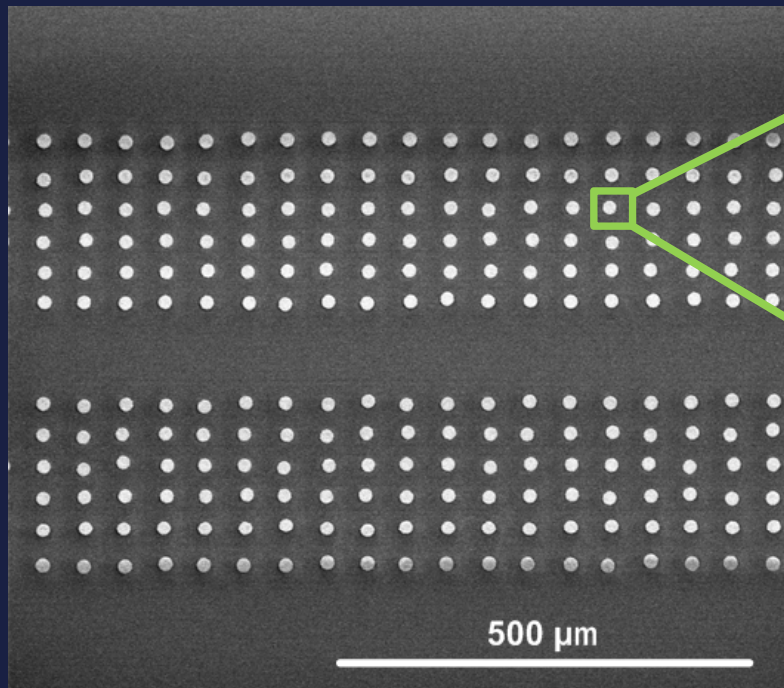
FormFactor NanoPierce™ Contact Solution



NanoPierce™ Contactor
1104 Interconnects on 40μm x 50μm grid

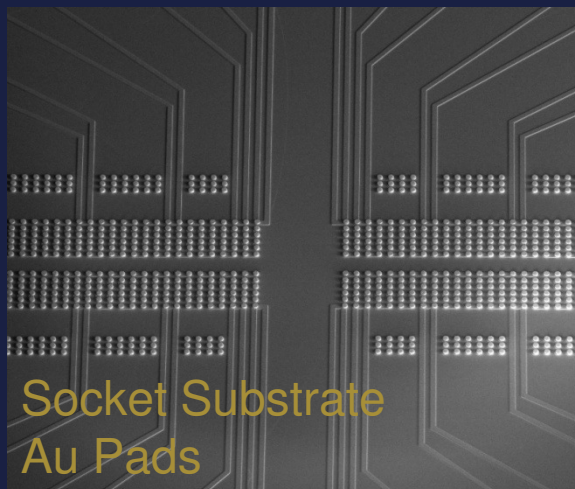
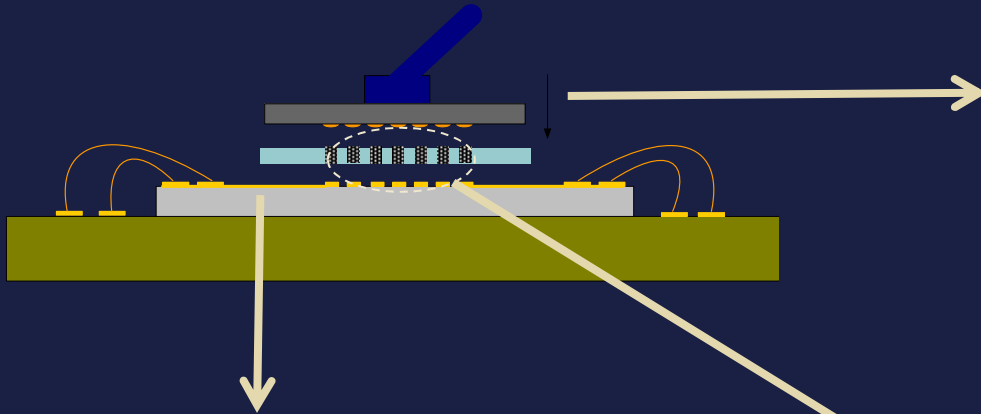
- FormFactor proprietary NanoPierce™ contacts are highly scalable
- Compliant contacts have lateral stability and can be individually compressed
- Thousands easily fabricated at very dense pitch

Contact Surface of NanoPierce™ Contact

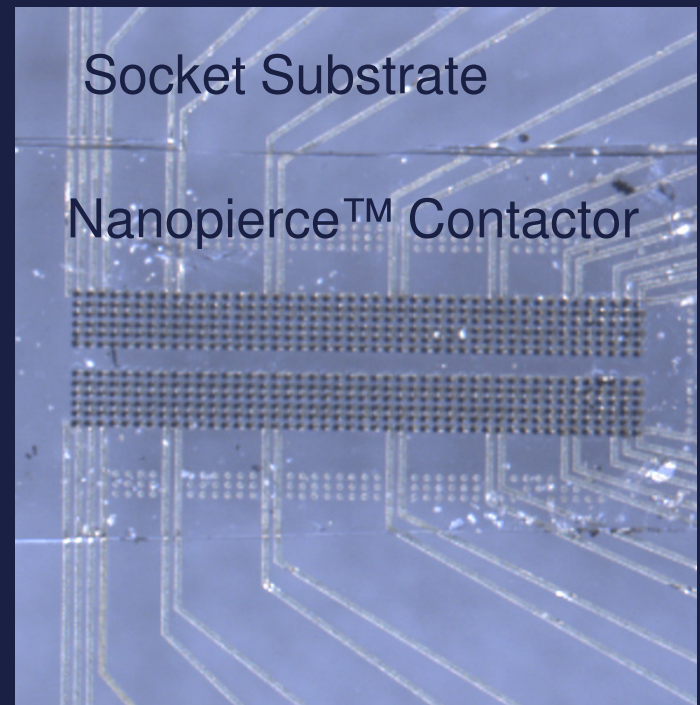


- Metal NanoFiber contacts with many contact points in one pad
- Force per contact ~0.5g with 25 microns compliance
- Estimated inductance per contact 0.1nH

Test Vehicle for NanoPierce™ Interconnect Socket Emulation

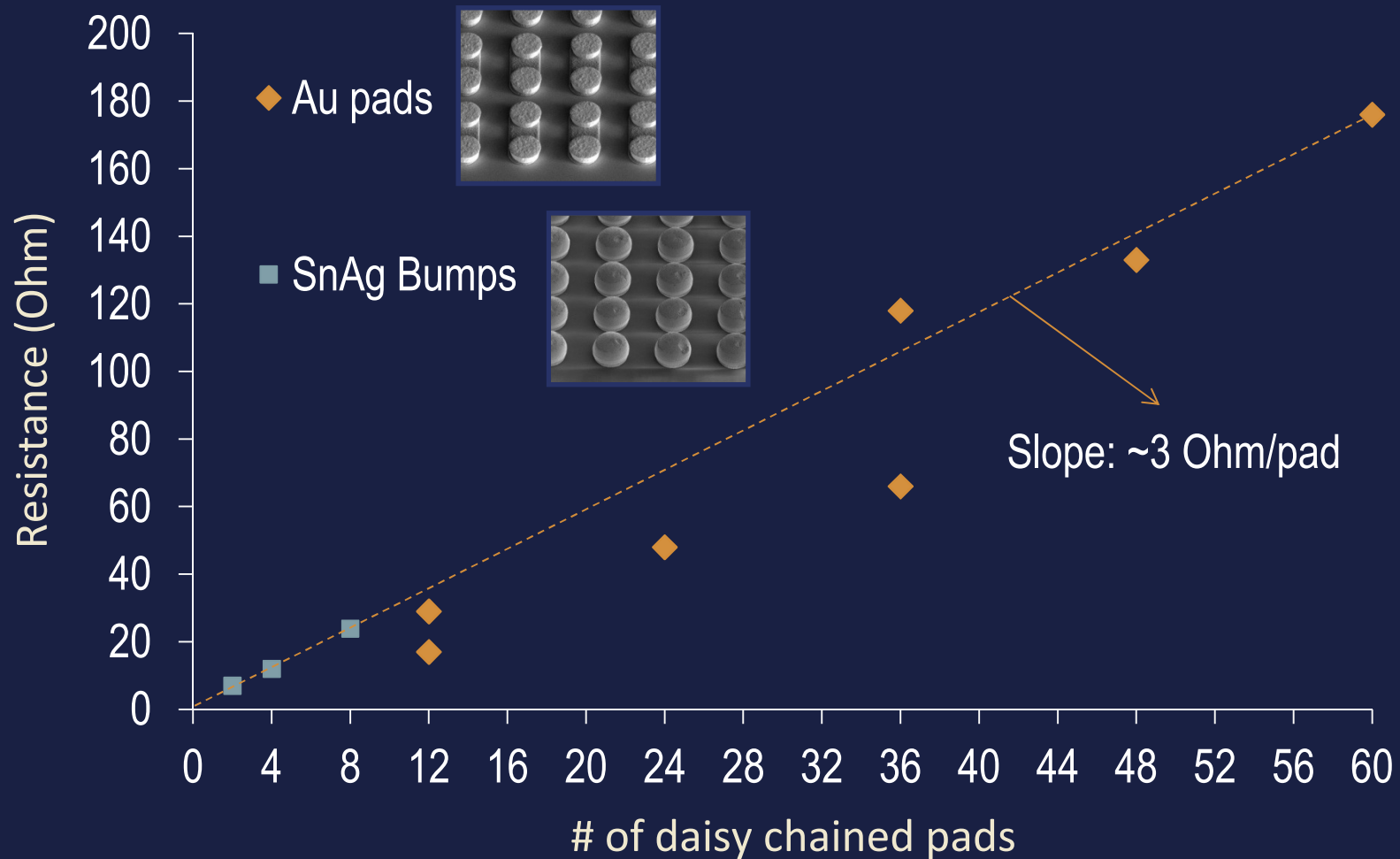


NanoPierce™
Interconnect
Placed on
Socket
Substrate



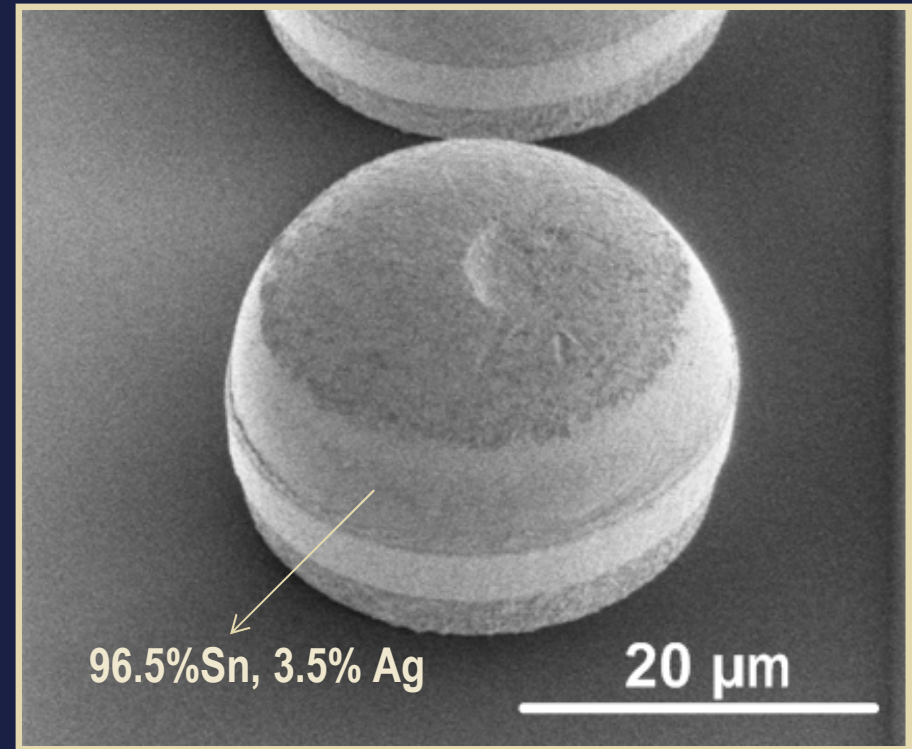
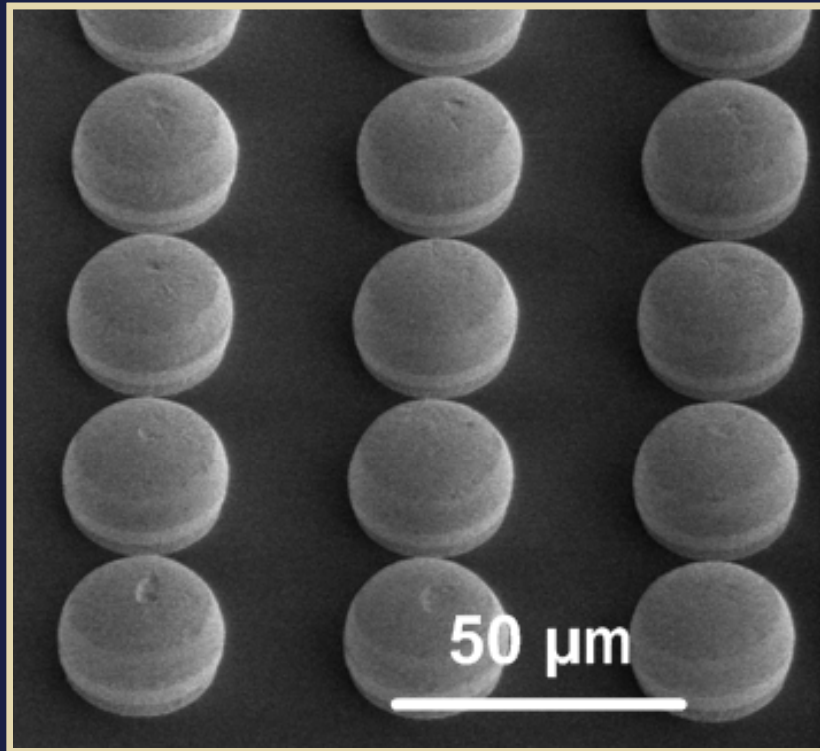
Daisy Chain Interconnection at
40x50 micron Array Pitch

Test results on Au pads and SnAg bumps



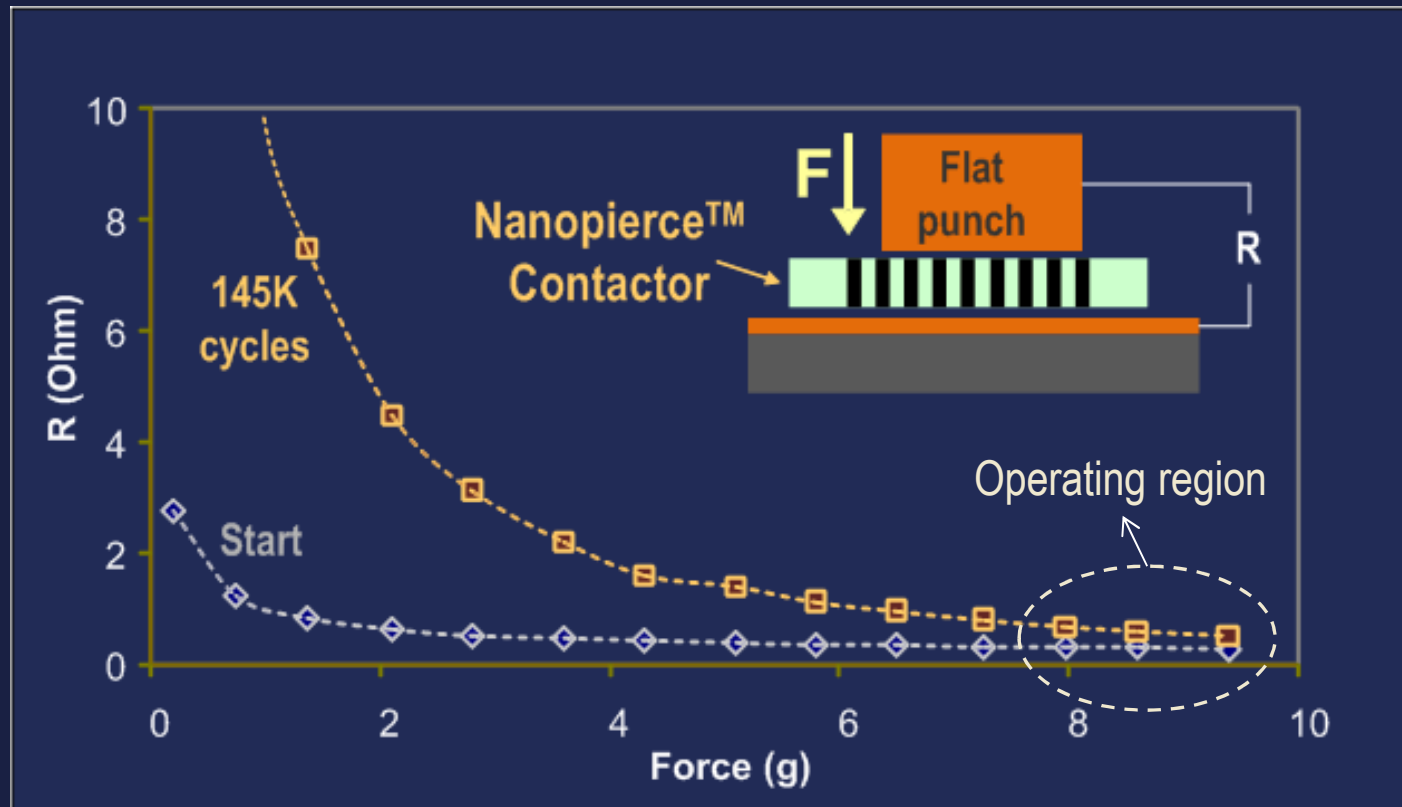
- All channels/quadrants of wide I/O pattern can be tested simultaneously
- Resistance is dominated by bulk resistance of Nanopierce™ contactors

SnAg Bump damage after 1 Touchdown



- Small damage on SnAg bumps.
- Not expected to cause joining issues.

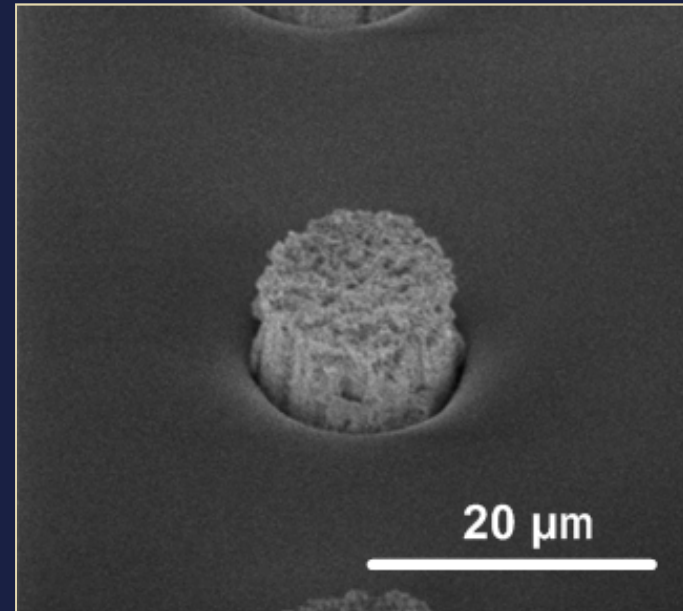
Cyclic testing on Sputtered Au Surface



- 145K cycles @ 25 μ m over travel (bulk testing of 10's of contacts)
- Some increase in force for contact, but no significant change in resistance at operating region.

Cyclic Test Results

- NanoPierce™ contactor after 960K cycles
- No significant change in contactor shapes.



- Scrub marks after 25000 cycles on 1000Å sputtered Au surface.
- No marks detectable at 1-100 contact cycles

