



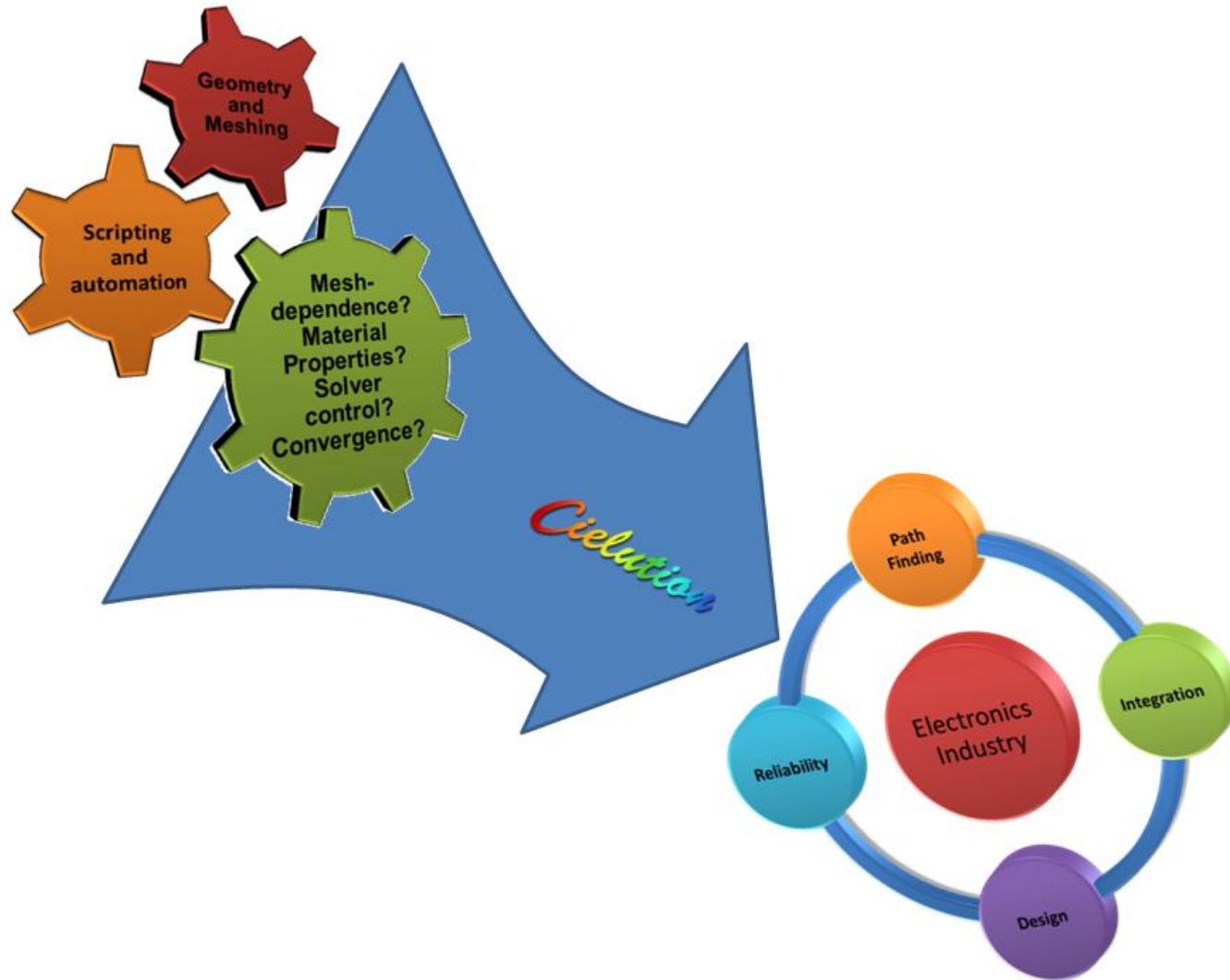
Cielution LLC Products Summary

CielSpot

CielSpot CTM

CielMech

Cielution Vision



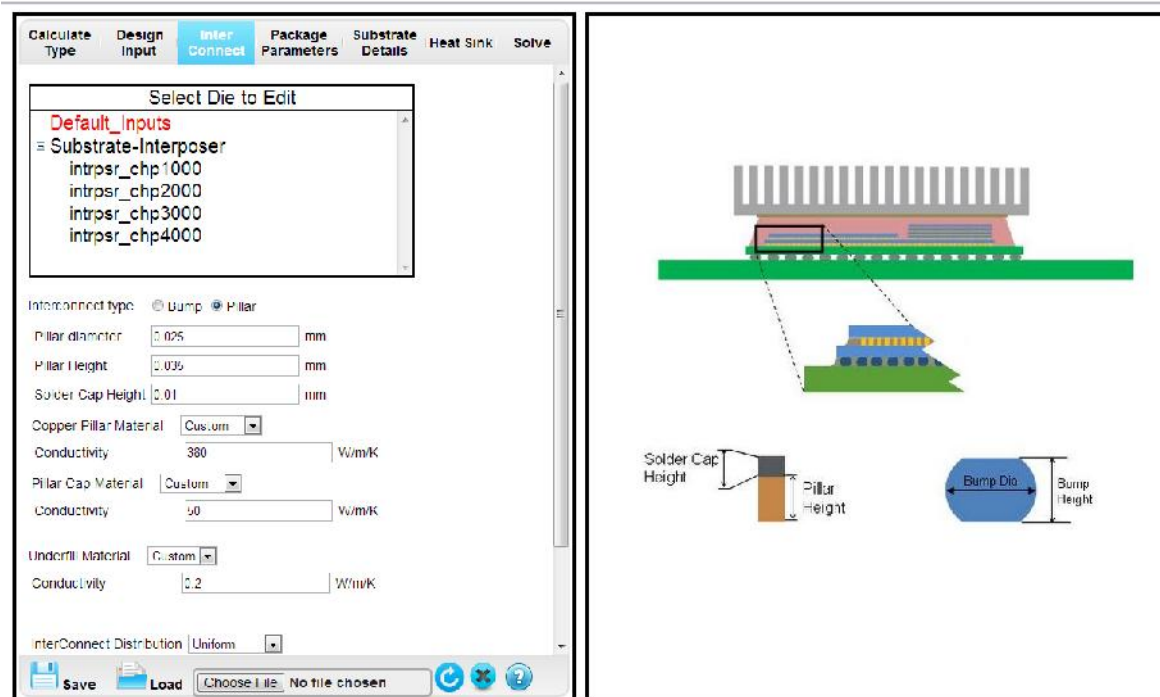
Cielution

Cielution Products

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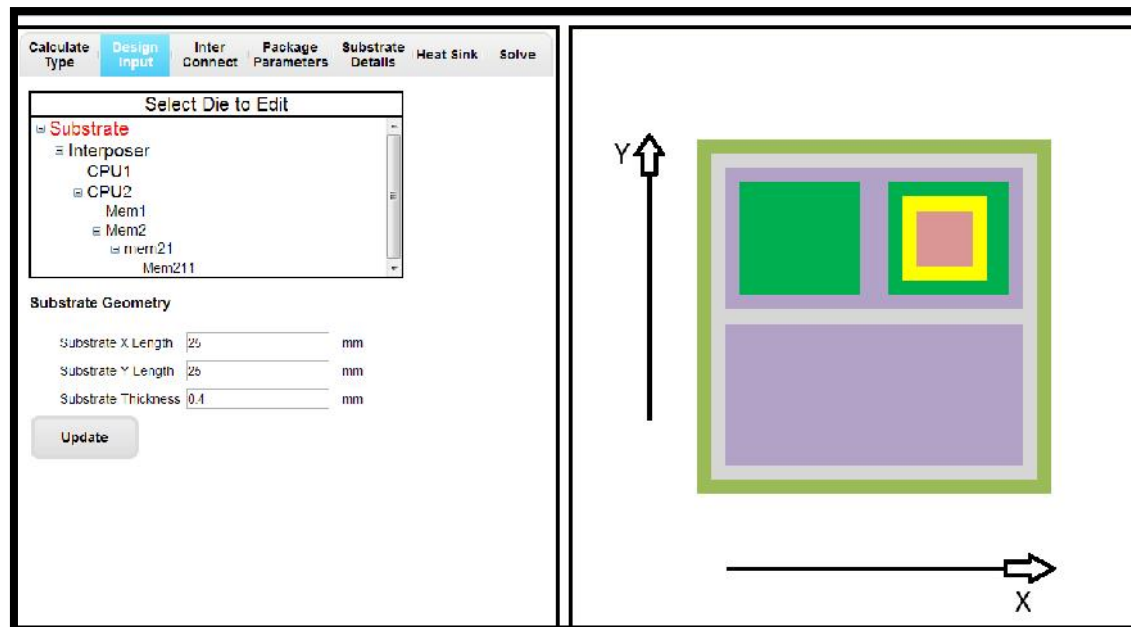
Cielution Product Pipeline

- **CielSpot™**
 - Package Thermal Modeling
 - Package Compact Model Generation
- **CielSpot-CTM™**
 - Thermally Aware IC Layout
 - Traditional Packages
 - 3D Stacked Assemblies
- **CielMech™**
 - Thermo-Mechanical Analysis of Assembly
 - Warpage Mitigation
 - Packaging Yield Enhancement
 - Interconnect Reliability

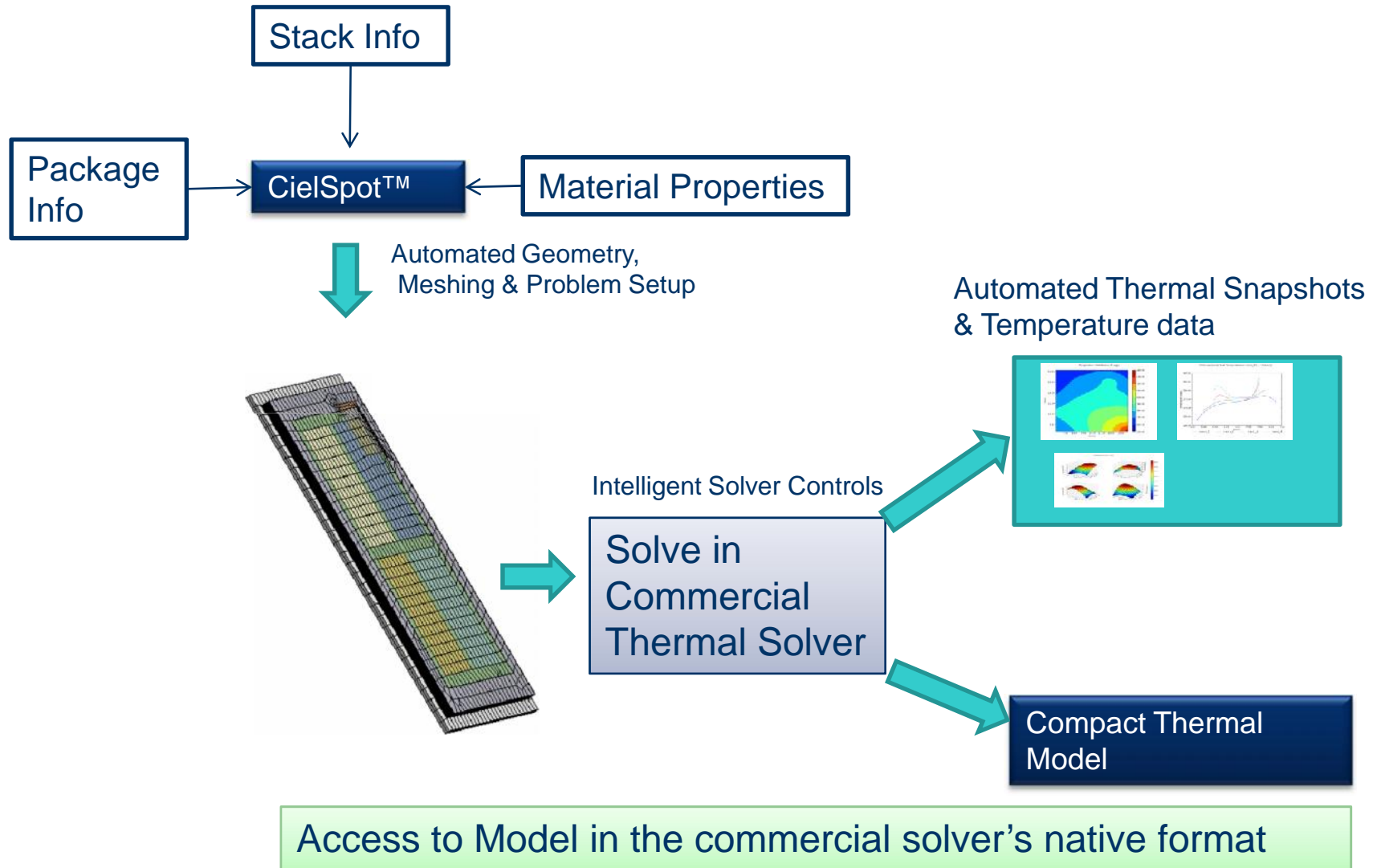


Product Roadmap – CielSpot™

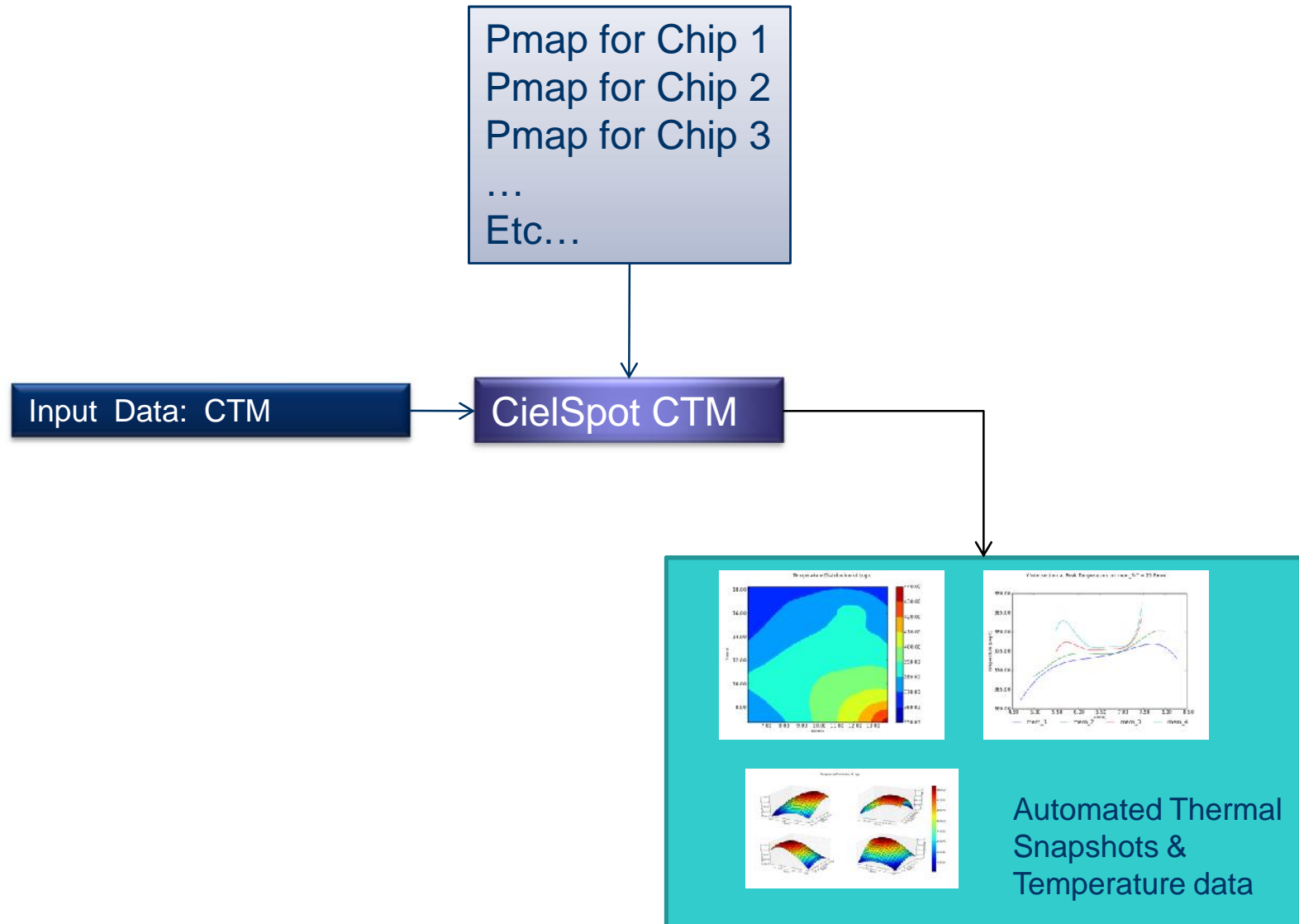
- Cielspot – Thermal Co-design tool for monolithic & 3D packages
 - User friendly temperature prediction of monolithic or stacked dies carrying distributed power.
 - Compact model generation for studying the effect of various power maps within seconds.
 - Validated - very accurate
 - Available to customers



CielSpot: High Level Workflow

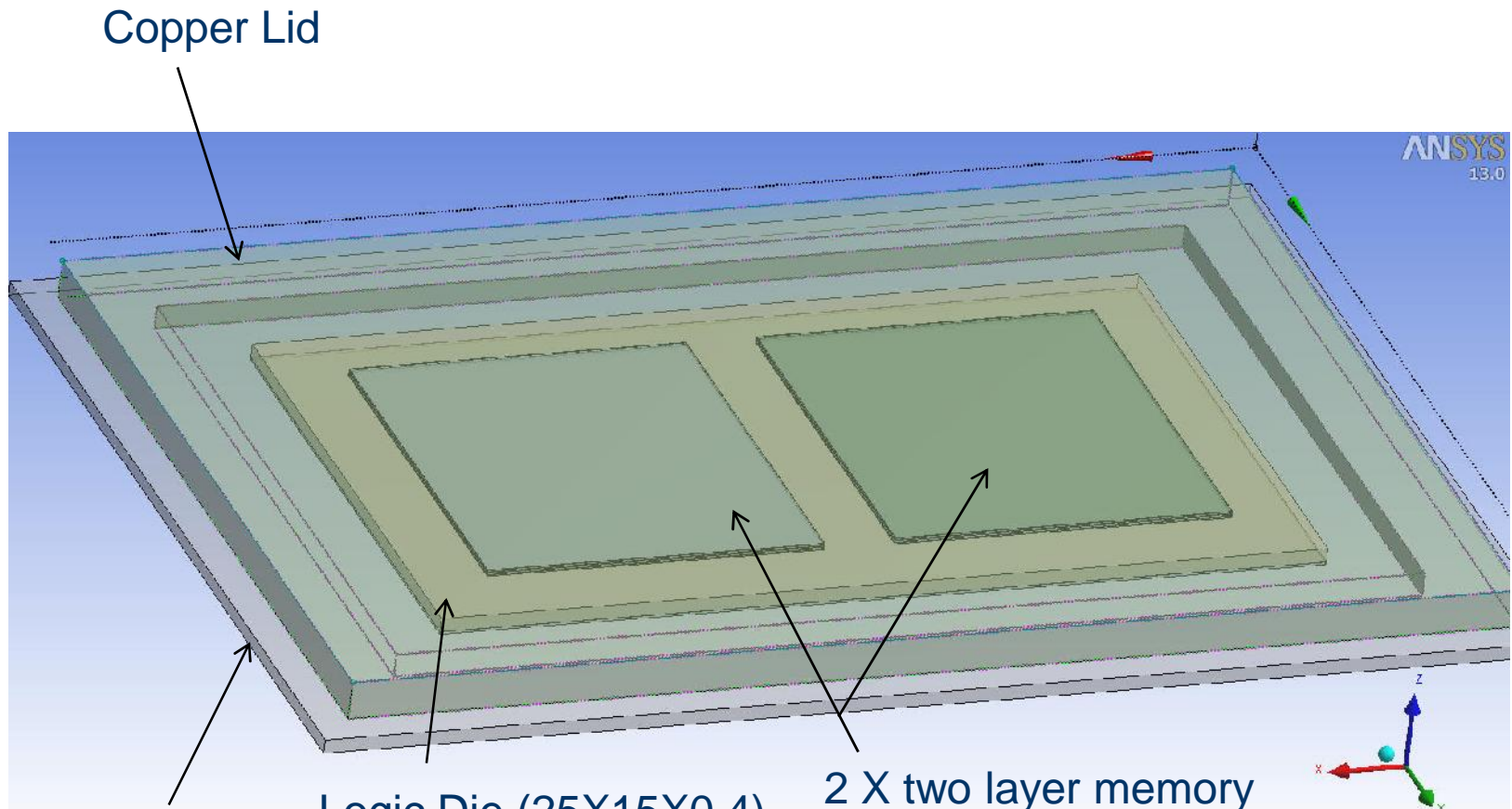


CielSpot-CTM Usage: Compact for Fast Solve Without CFD/FEA



CielSpot© Validation

Package used for Validation



Copper Lid

Substrate

Logic Die (25X15X0.4)

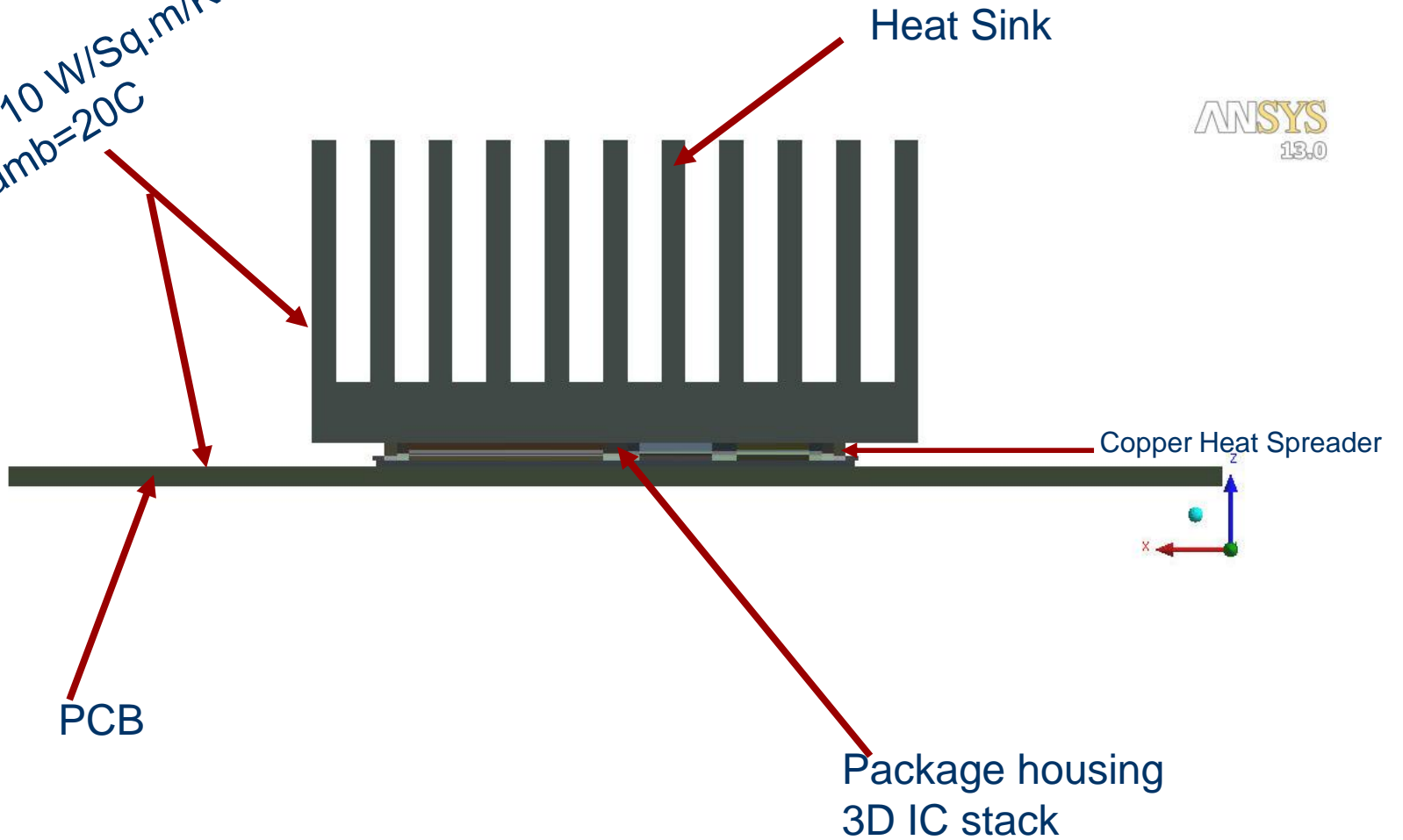
0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04

2 X two layer memory Stacks (9.5X11X0.05)

0.04	0.04	0.04	0.04	0.04
0.04	0.04	0.04	0.04	0.04
0.04	0.04	1	0.04	0.04
0.04	0.04	0.04	0.04	0.04
0.04	0.04	0.04	0.04	0.04

Packaging & Cooling Scenario I

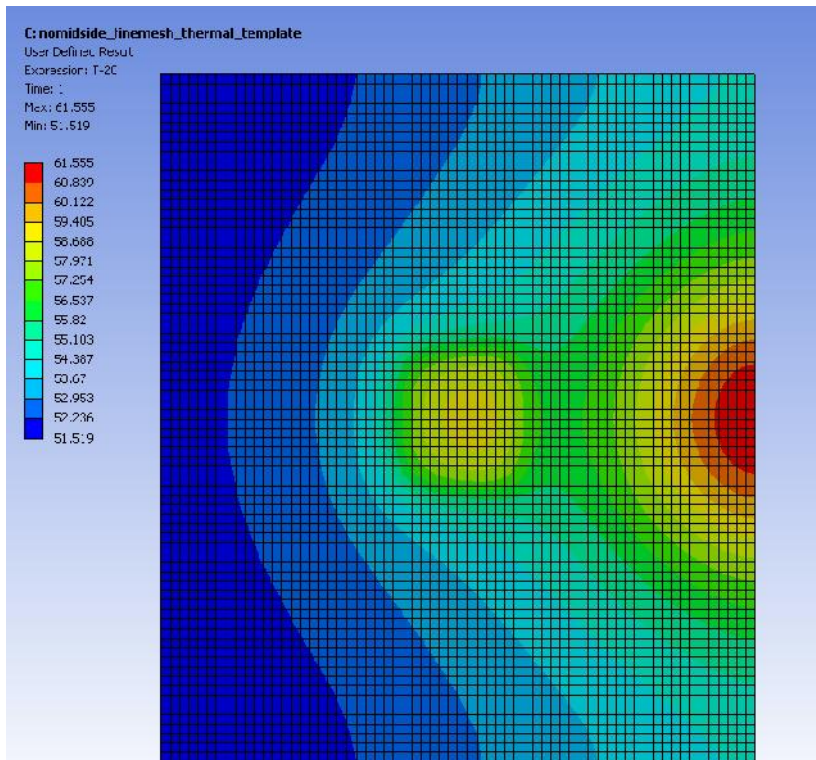
$h = 10 \text{ W/Sq.m/K}$
 $T_{amb} = 20\text{C}$



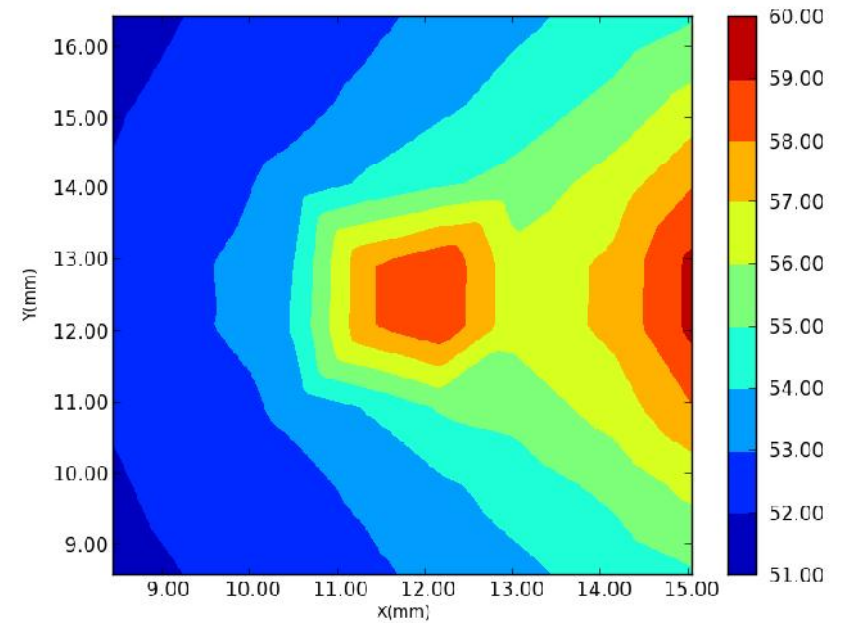
ANSYS
13.0

Validation Results

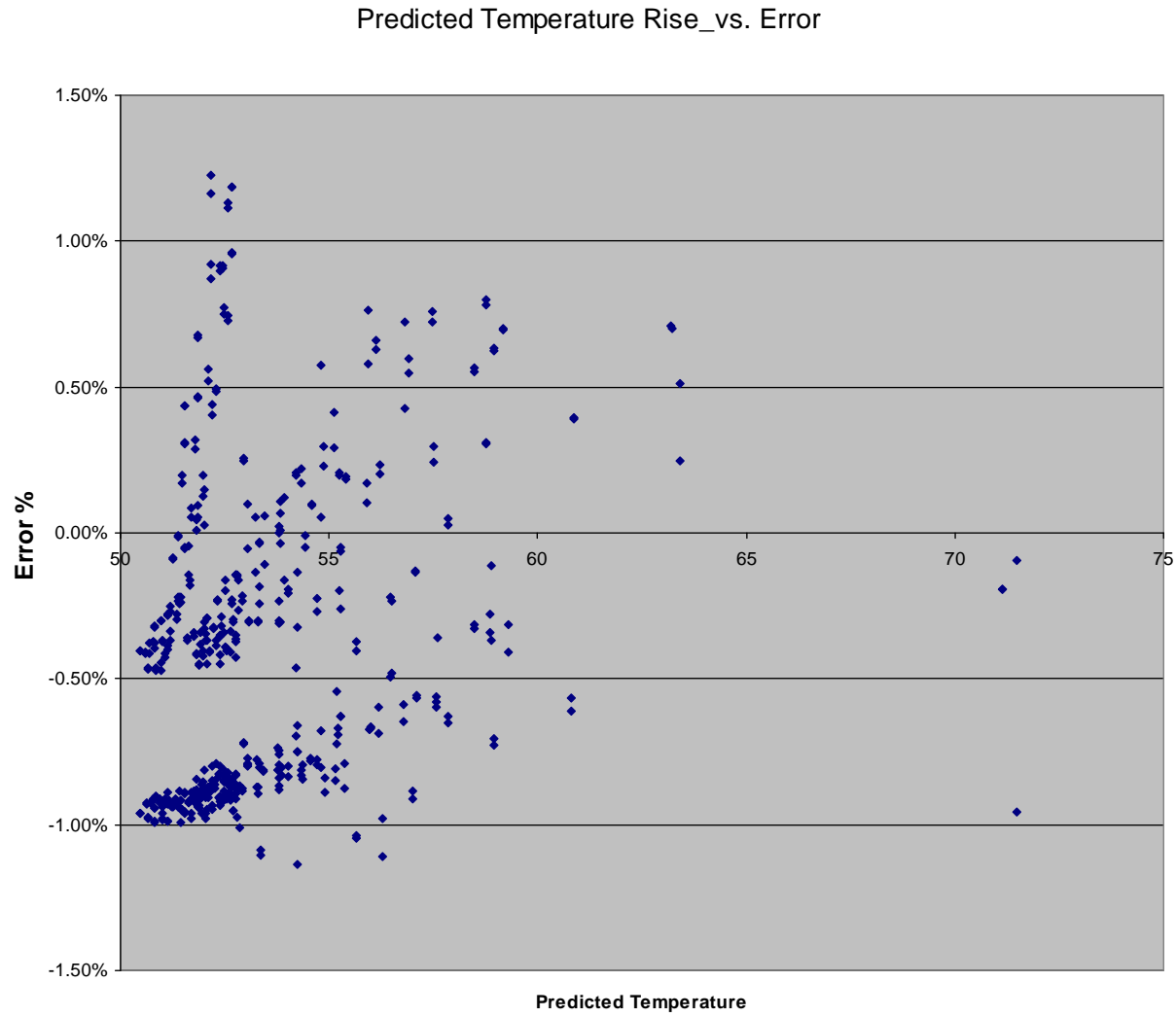
FEA (ANSYS) Prediction of Temperature Distribution on Memory-I



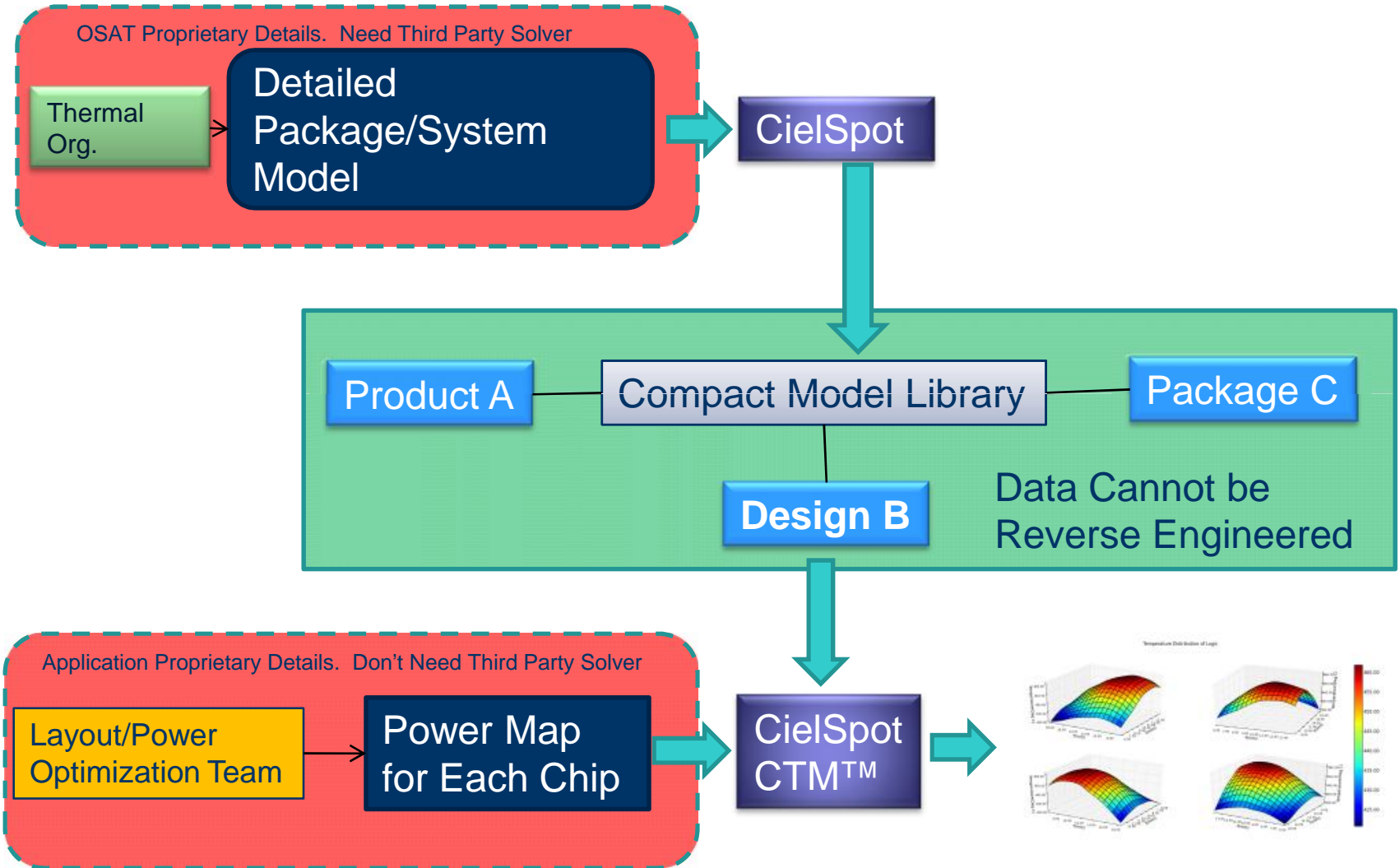
CielSpot-CTM Prediction of Temperature Distribution on Memory-I



Distribution of Errors



Collaborative Thermal Modeling using CielSpot™

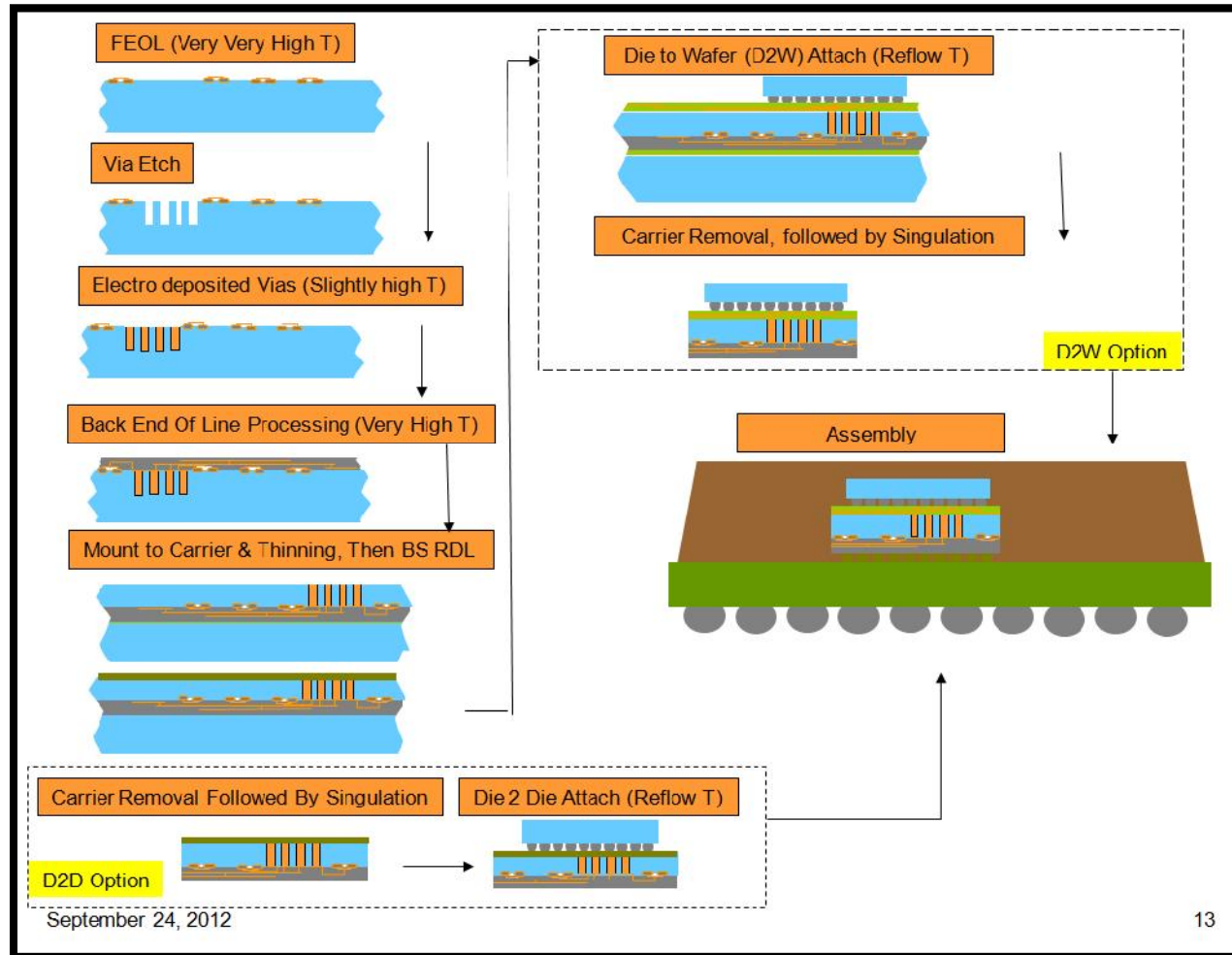


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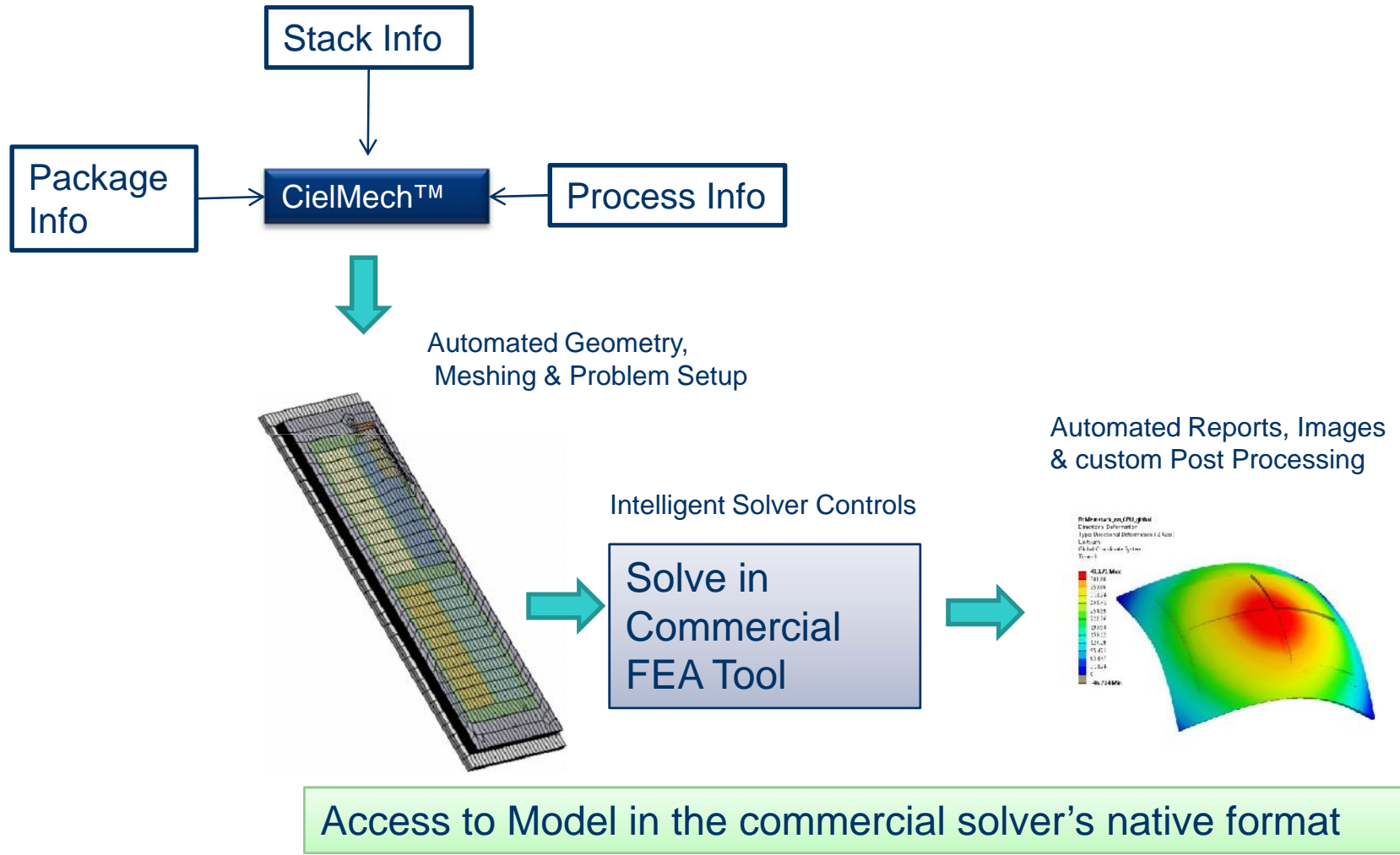
CielMech™

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D2D Assembly Workflow (1)



CielMech: High Level Workflow

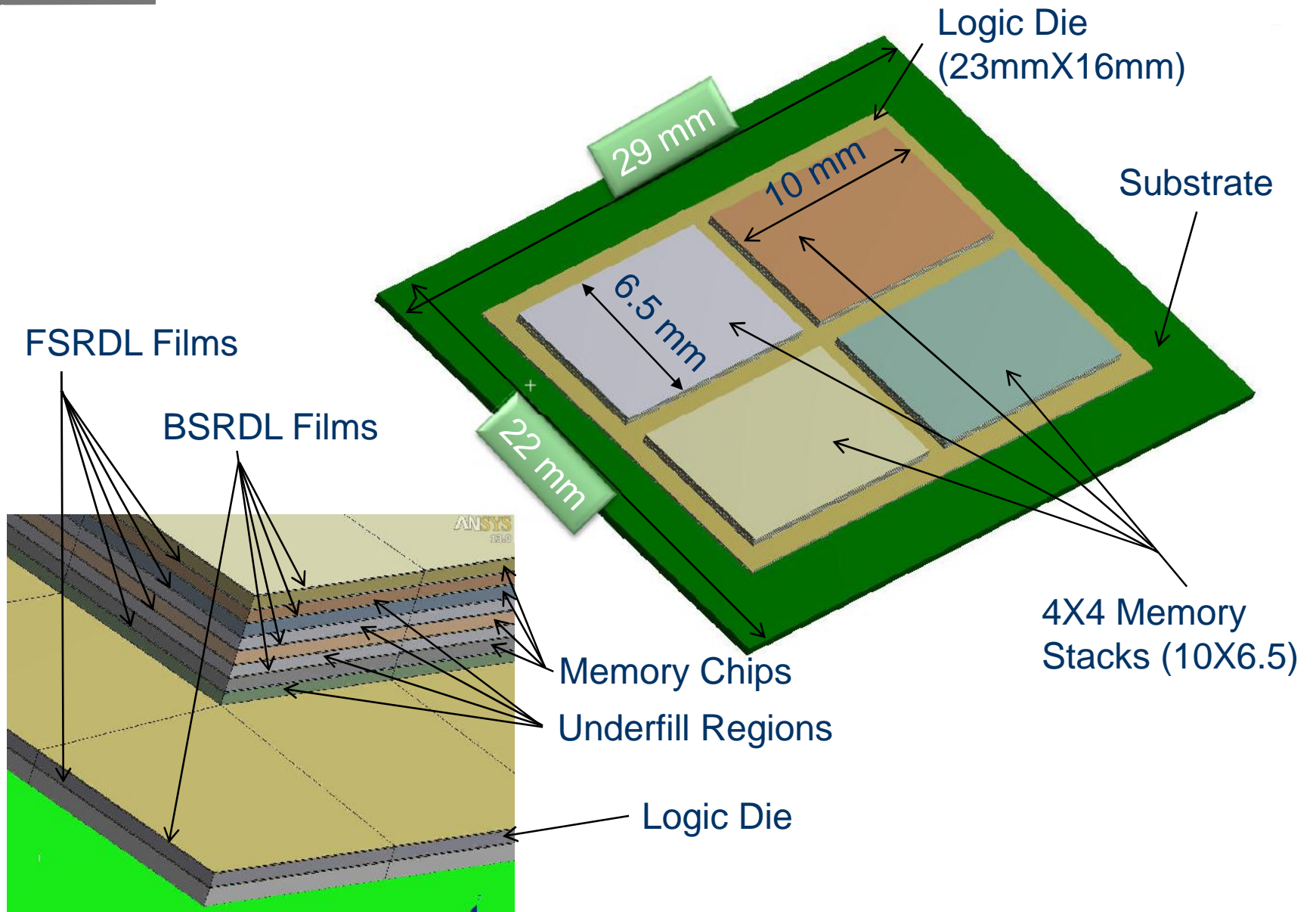




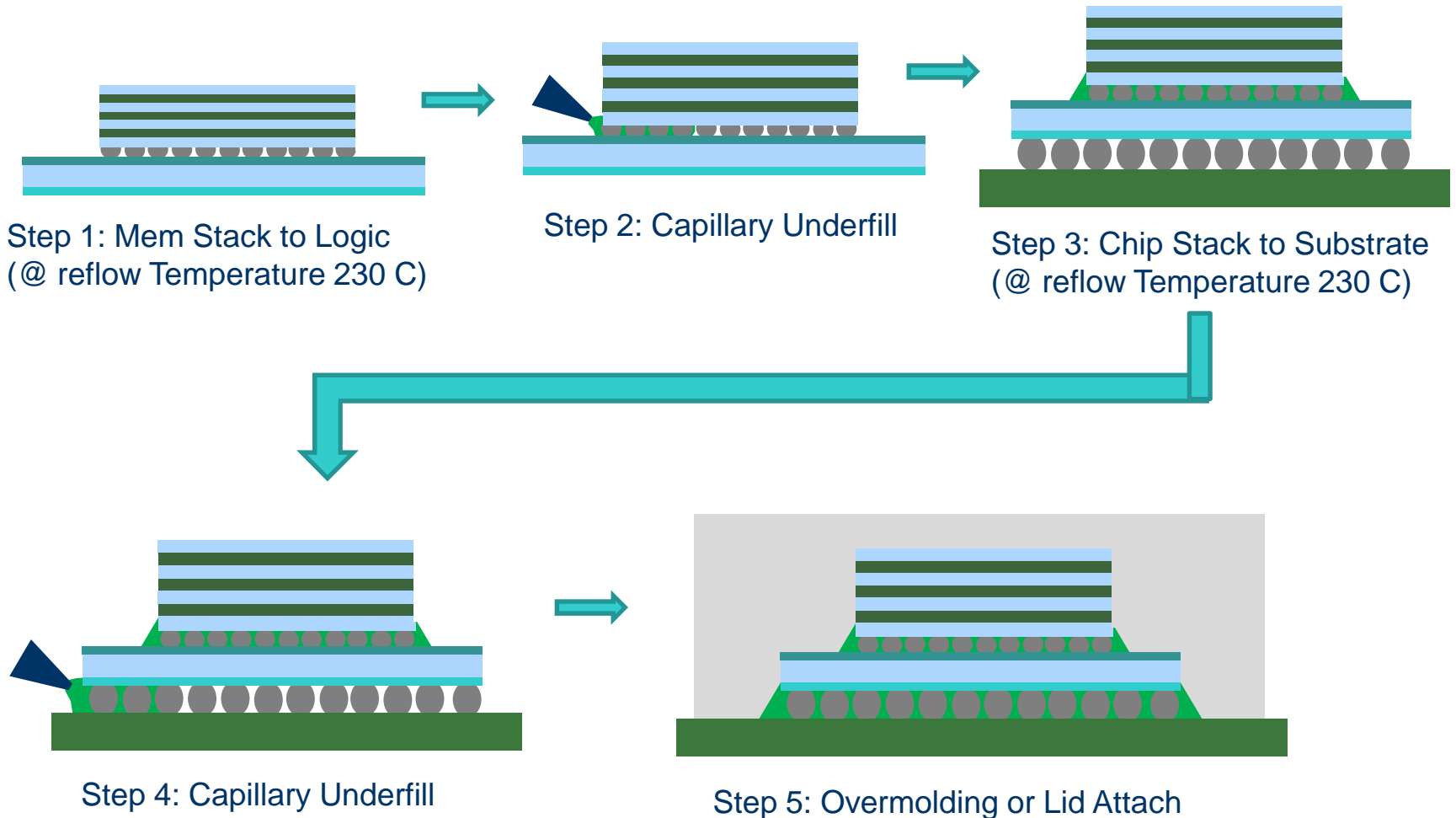
Chip Stacking Case Study

ECTC 2013 Paper
Summary

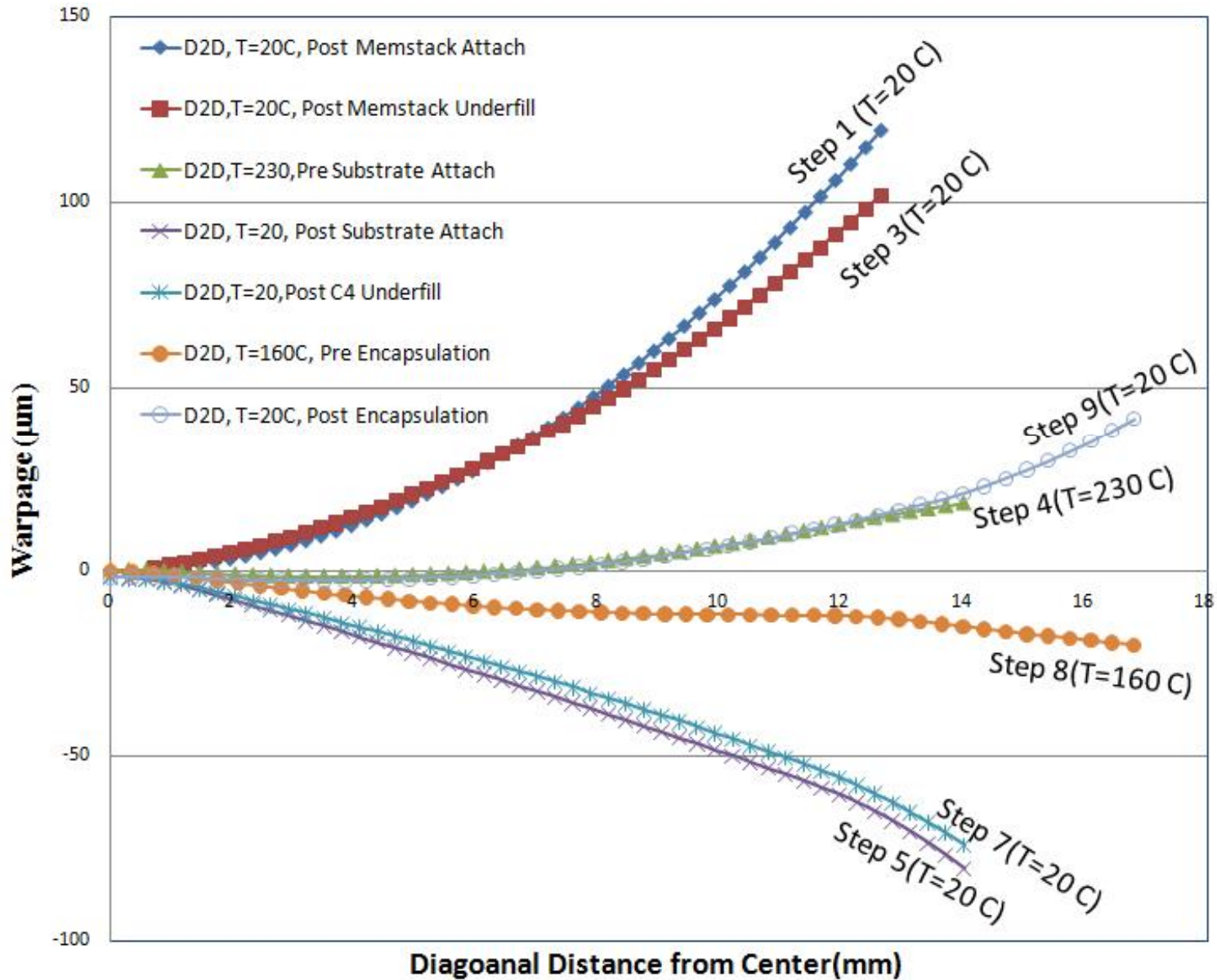
Stack up Description



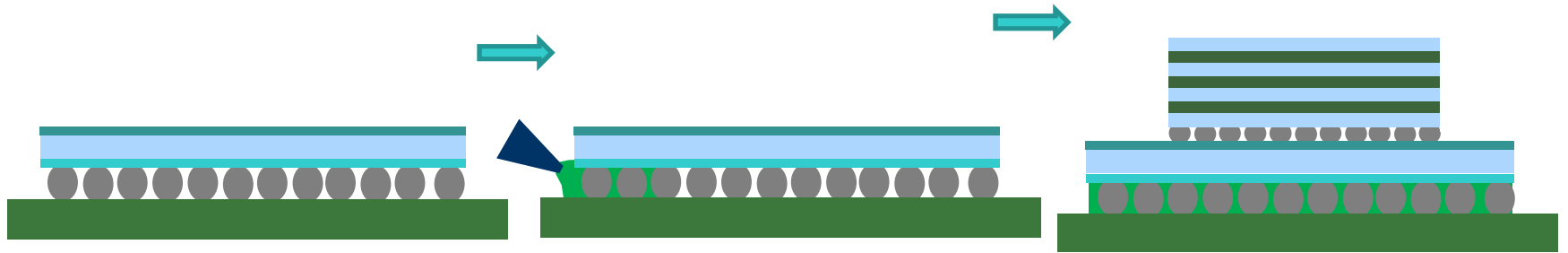
3D Assembly Flow I: D2D



Warpage Evolution for D2D Flow



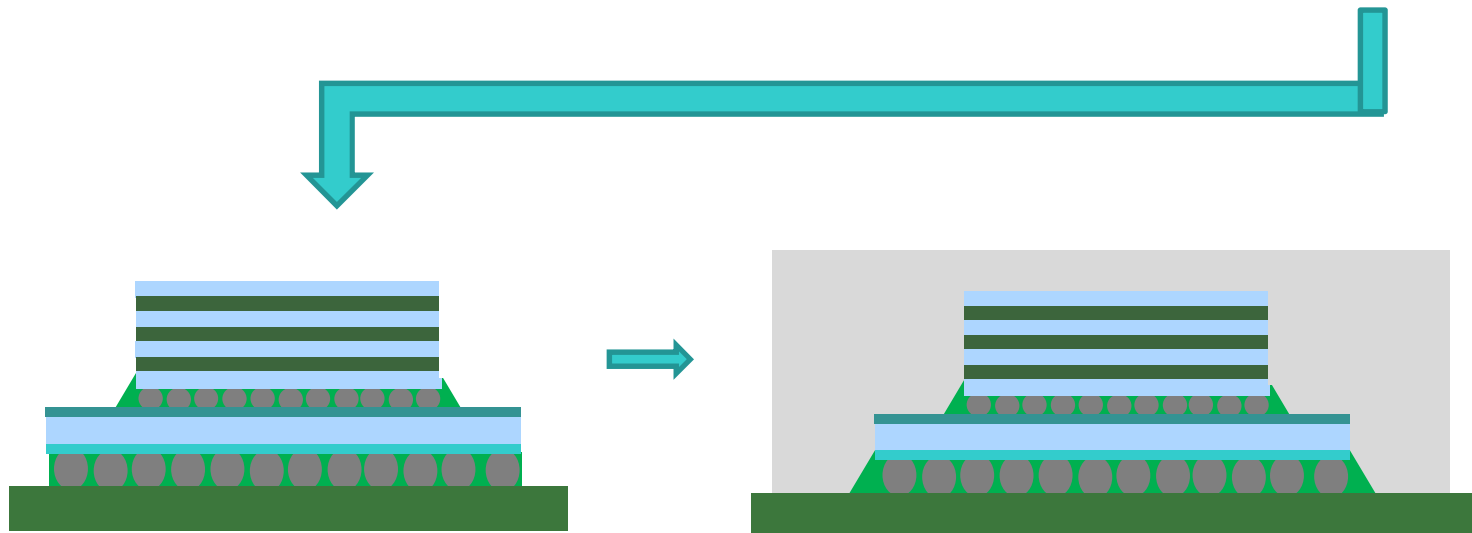
Assembly Flow II: P2D



Step 1: Mem Stack to Logic
(@ reflow Temperature 230 C)

Step 2: Capillary Underfill

Step 3: Memory Stack Attach



Step 4: Capillary Underfill

Step 5: Overmolding

Warpage Evolution for P2D Flow

