3D-IC System Verification Methodology: Solutions and Challenges

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***Abstract*— A verification methodology for 3D-ICs is presented, including connectivity checking and parasitic extraction. An example was given to illustrate a true 3D-IC stack verification using a GDS based flow. The new challenges were presented and the development efforts to respond to those challenges were identified.**

***Index Terms*—3D-IC, interposer, TSV**

I. Introduction

The performance and cost savings for moving toward through silicon via (TSV)–based three-dimensional (3D) integration motivations have been identified [1]-[2]. 3D integrated circuit (IC) technology enables shorter critical interconnections, which will reduce both the delays and power. In addition, it will allow easy reuse of IP blocks, heterogeneous technology integration, and a reduction of the form factor.

Technological issues for 3D IC technology include TSV formation, die thinning, thinned die handling, assembling and testing; but, according to the foundries' recent announcements [1], the technology is at a stage that will allow for significant commercialization in the next few years.

Typical applications include image sensors, memory stacking, logic on memory and FPGA. We expect to see applications with heterogeneous die stacking and applications where the logic is split between the dies in several years. These applications will bring new challenges in the design and verification of 3D systems.

3D die stacking comes in different configurations including silicon interposer–based integration (called horizontal or 2.5D integration), vertical die to die stacking (also called 3D stacking), and a range of mixed configurations. An interposer-based stacking gained popularity last year because of several attractive applications [4] as well as its technological feasibility. It might not be sufficiently effective for other applications, however, such as the memory on logic [5] or the logic splitting application, where the logic is split between two or more dies that are then put on top of each other for shorter interconnections. Also memory can be split in such a way that read-write logic is on one chip while the cells are on the other. A true 3D stacking is needed for maximum performance in those applications.

The three largest EDA companies are taking an evolutionary, rather than a revolutionary, approach in developing the 3D IC design tools. This appears to be a good decision because the technology, the rules and the standards are still evolving. The main EDA challenges are expected in the design space exploration [6], automatic across-die design partitioning, placement and routing, thermal and stress management, and 3D stack testing.

Regardless of design style and methodology, physical verification is a necessary step to accurately verify design rule compliance, 3D stack LVS checking across the die parasitic extraction and simulation. Existing verification flows include the use of DRC, LVS and extraction to verify the connectivity of multiple stacked dies [7].

At the present stage of technology development and 3D IC applications, it is assumed that there are no interactions between the TSVs, and a model for a single TSV is provided by the foundries. For verification purposes, TSVs are treated as an LVS device (GDS based flow) or as a Via (LEF/DEF based flow), and the provided TSV model is used for downstream simulation. This assumption, however, may not hold true as the technology advances and the TSV densities and frequencies become high, requiring accurate modeling and extraction of the interactions. Significant research effort has been put into this area recently [8]–[10] and it is expected to intensify in the coming years. This new methodology would require more accurate process description, accurate frequency dependant modeling and appropriate flow development to take advantage of the modeling accuracy.

We discuss various verification flows and present the solutions that allow for accurate verification of current 3D designs in this paper. We also point out the challenges that come with the new applications and identify development efforts needed to respond to those challenges.

The paper is organized as follows. Section 2 introduces typical configurations and the ways of their description for the design and verification purposes. Section 3 presents the verification flows for true 3D stacked systems and the interposer-based stacking including both analog and digital (GDS-based and LEF/DEF-based flows). Section 4 provides one detailed example illustrating current methodology and flows. Section 5 identifies the issues related to the current methodology as well as the needs and directions for future 3D verification work. The last Section is Conclusion.

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II. Die Stacking Configurations and Descriptions

TSVs that connect the front side metal and the back side of the chip must be used to stack the dies on top of each other efficiently, as shown in Figure 1.

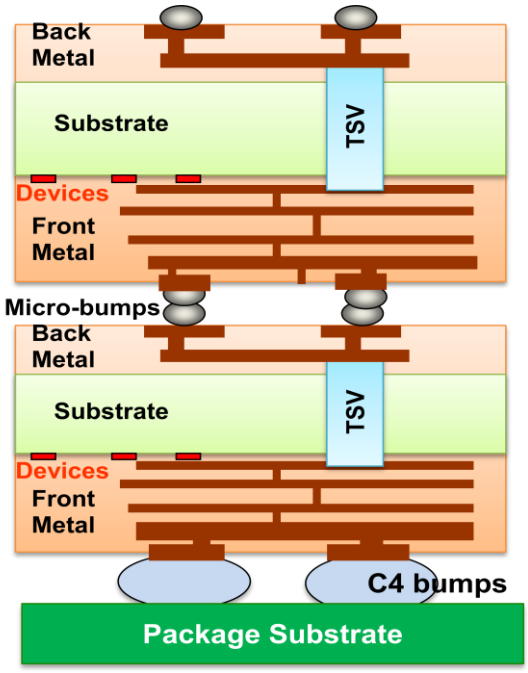

Figure 1. Double-sided die with a TSV connecting the front side metal1 layer and the back side metal1 layer.

There could be one or two redistribution layers on the back side. Alternatively, the TSVs can be directly connected from the front side metal1 to the microbumps on the back side of the chip to reduce the cost.

The chips can then be connected back to front, back to back or front to front. Typically the micro bumps or the copper pillars are used to connect the chips. A back-to-front configuration is shown in Figure 1. These configurations result in so-called true 3D designs. They also allow for an increased performance and the reduction of power. The stack configuration, as shown in Figure 1, represents the initial approach, proposed by the design houses and the foundries, to make efficient 3D IC systems. The typical approach uses a "via middle" process, i.e., the TSV is formed after FEOL and before BEOL. However, there are technological challenges to fabricating TSVs, with this approach; for example, a shift in the transistor characteristics could be introduced which would significantly and unpredictably affect the system performance.

Consequently, the technology to stack the chips using the interposers (made of silicon or glass) was proposed to avoid this issue and to not have to change the original to make a safe space for the TSVs connections. In this approach, the dies are flipped and connected to the interposer, typically by using the micro-bumps as shown in Figure 2.

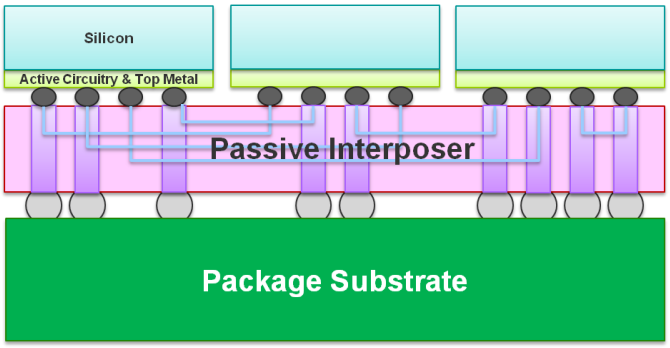

Figure 2. Interposer based configuration, with flipped chips, microbumps to connect the die to the passive interposer with no devices, TSVs in the interposer only, with a C4 bump to the package substrate.

No TSVs are needed on the active dies. The TSVs are fabricated on the passive interposer to connect the chips to each other and to the package beneath. By using the interposers, the technological challenges are significantly reduced but at the expense of the longer interconnections between the chips.

This configuration is suitable for FPGA designs, such as the Virtex-7 FPGA by Xilinx [11], in which a large FPGA can be partitioned so that only communication between the neighboring chips on the interposer is required , thus reducing the potential problems with long interconnection delays. In addition to the reduced stress, the interposer-based configuration also simplifies the power distribution problem, which can be very significant in true-3D stacking.

The configurations for the stacks should be properly described to assist with the design and verification. The emphasis is on the precise description of the interfaces (chip-to-chip or chip-to-interposer) so that an appropriate verification process can be done efficiently.

A configuration file, used to describe a 3D stack, typically contains a list of dies with their order number, the information of the die position, rotation and orientation, as well as the location of the GDS files and associated rule files and svdb directories. The interface type and the rules (DRC and LVS) are also specified in the interface rule files.

For parasitic extraction of the chip interfaces, descriptions of the dimensions and electrical characteristics of the interface materials (micro-balls, cooper pillars, bonding material properties, etc.) are needed, as well as the number of layers that should be taken into account from the neighboring dies (up and down) for parasitic extraction.

III. Stack Verification Methodologies

A 3D-IC stack verification, regardless of the configuration, includes DRC, LVS, parasitic extraction (PEX) and simulation. The approach taken today is to first do DRC/LVS/PEX of the individual dies separately and then to consider the interfaces. As for the interfaces (between the vertically stacked dies, as well as between the dies and an interposer), a separate GDS is formed that consists of the interface layers, and then DRC and connectivity check is performed on a newly formed GDS. Based on stack information (die order, *x*,*y* position, rotation and orientation

etc.), provided in a configuration file, the tools automatically perform DRC and connectivity check of the entire stack. The text labels should be inserted at the interface microbump or cooper pillar locations to perform the connectivity check.

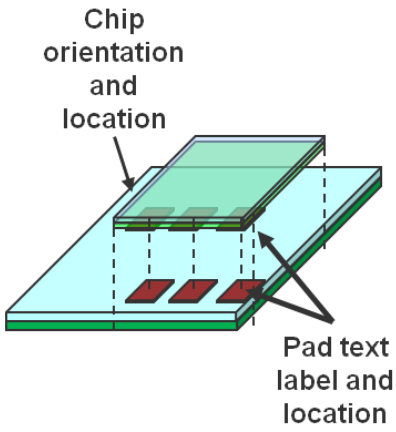

Figure 3. Text labels inserted.

Depending on whether the flow is analog or digital, either dynamic or static timing analysis is performed andsome LVS and extraction requirements are different. There are also some differences specific to the verification of the interposer based stack vs. vertical 3D stack.

In the analog flow, TSV is described as an LVS device, and there is no need for TSVs extraction. When calibration and subsequent extraction is done, only the front and back side metal layers are calibrated and extracted. A Spice model of the TSV circuit (R,C,(L)), provided by the foundries, is used in simulation.

In a digital flow, TSV is typically treated as a via, not as a device (cell). This requires a special approach. Namely, calibration with a TSV profile generating a simple R,(C) model for the TSV must be done, which can then be used in simulation if high accuracy is not required. For improved accuracy, a circuit is provided by the foundries, and the simple model generated during calibration is replaced with the provided model for more accurate static timing analysis. Another option in the digital flow is that a TSV could be characterized as a cell for timing and/or power and then used in static timing and power analysis. However, there are not yet providers for those library elements and a typical digital flow is as already described above.

In the verification of the interposer-based stack, the dies do not have TSVs and their DRC/LVS/PEX is done for the individual chips as usual. LVS of the interposer has to be done separately.

In a GDS flow, the interposer TSVs are treated as LVS devices, and verification is done pretty much as described for the case of a chip with double-sided metal and the TSVs.

In a LEF/DEF flow, some additional steps are needed because TSV is treated as a via, and the interposer does not have active or passive devices. For completing proper interposer verification, Fake devices (typically resistors) are inserted at the bump locations, LVS and extraction is performed, and then the fake devices are filtered out before simulation.

The interface between the die and the interposer is checked the same way as the interface between the die to make sure there are no the rule violations and that the proper connectivity is established for the whole stack.

There is still no need for true LVS of the stack, and the 2.5D approach described is sufficient for the present applications.

For the simulation, individual chip netlists as well as a 3D stack top level netlist are produced and are used based on the capabilities of the available simulators (Figure 4).

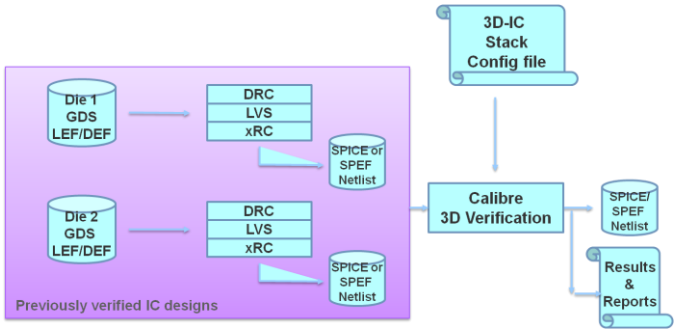

Figure 4. 3D-IC verification flow.

Once the applications that require logic splitting between the die hit the market, this situation will be changed and will require a different approach.

IV. Example(s)

A 3D-IC was designed using a 65-nm technology, with a logic die, a memory die and microbumps connecting the two.

The logic die on the bottom consists of six top metal layers, an active layer with MOS devices, TSVs and one back metal layer. The logic die is oriented upside down, with the active layer on the bottom and the back metal on the top.

The memory die lies on top of the logic die, and consists of six top metal layers and an active layer with MOS devices. It also is oriented upside down.

Figure 5 shows the orientation of the logic and memory die.

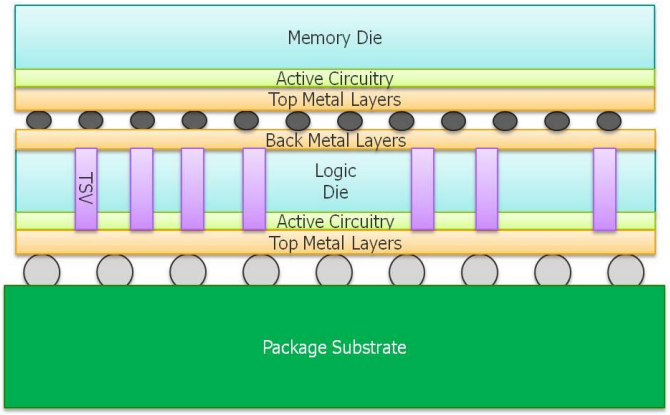

Figure 5. 3D-IC with the logic die on the bottom (upside down), and the memory die on the top (upside down). Microbumps connect the two dies, and flip chip bumps connect the logic die to the package substrate.

The TSV on the logic die connects the top side metal 1 layer to the back side metal1 layer. The back metal pads are then directly connected to the copper pillar microbumps.

Calibre DRC was run on both the logic and memory die using standard DRC rule decks. Additional rules for TSVs and microbumps were used to check the manufacturability of the TSVs and microbumps.

Calibre LVS was used to check the connectivity of the logic and memory dies individually, with the TSVs recognized as intentional devices.

Then the top metal layer of the memory die, and the back metal layer of the logic die were merged together to check for connectivity errors. The landing pad for both sides of the microbump needs to be correctly aligned. The interface connectivity was checked to ensure that the proper nets were connected through the microbumps and that the alignment of the logic and memory dies is correct.

The Calibre xACT 3D field solver was used to extract the parasitics. A new extraction rule file was generated with xCalibrate to include the back metal stack. The capacitance of nets that belong both on the logic and memory die was calculated and broken down into all the constituent pieces to see the ratio of TSV and microbump capacitance versus on-chip capacitance. The TSV was treated as an LVS device, and a subcircuit provided by the foundry was used to model the TSV. The TSV-to-substrate capacitance is 75 fF. The microbump capacitance is estimated to be around 1 fF, based on a paper by Alam et al. [12].

All nets that are on both the logic die and the memory die that are connected by TSVs and microbumps were extracted. An assortment of ten various nets is shown in Table I. The total capacitance (coupling capacitance and capacitance to ground) is broken down into the different sections of the 3D-IC: top metal layers and polysilicon for the logic die, the TSV, the back metal on the logic die, the microbump, and finally the top metals and polysilicon on the memory chip.

Capacitance (F)	Mother Top Metal	TSV	Mother Back Metal	Microbump	Daughter Top Metal
NetA	7.52E-13	7.50E-14	1.09E-13	1.00E-15	3.70E-13
NetB	7.60E-13	7.50E-14	1.09E-13	1.00E-15	2.68E-13
NetC	7.20E-13	7.50E-14	1.09E-13	1.00E-15	8.78E-14
NetD	8.09E-13	7.50E-14	1.09E-13	1.00E-15	9.37E-14
NetE	6.91E-13	7.50E-14	1.09E-13	1.00E-15	2.66E-13
NetF	1.47E-13	7.50E-14	1.09E-13	1.00E-15	1.57E-13
NetG	1.36E-13	7.50E-14	1.09E-13	1.00E-15	1.55E-13
NetH	7.42E-13	7.50E-14	1.09E-13	1.00E-15	1.27E-13
NetI	7.60E-13	7.50E-14	1.09E-13	1.00E-15	1.87E-13
NetJ	7.23E-13	7.50E-14	1.09E-13	1.00E-15	8.71E-14

Table I shows that the significant portion of the capacitance in the nets still belongs to the top metals, both on the logic and the memory chips, but that the TSV contribution to capacitance can be quite high for smaller nets. Therefore, it is important to do simulation through the whole net chain, including logic top metal, TSV, logic back metal, microbump and memory top metal, to ensure that the signals are not being degraded and that the 3D-IC meets performance specifications.

V. New Challenges and Future work

The flows described in Section III and illustrated with one example in Section IV work well as long as the interactions between the TSVs, the TSVs and interconnects, TSVs and active devices, and other interactions are negligible. However, the interactions cannot be safely neglected anymore because of the increasing TSV densities [13], and they should be modeled and taken into account in simulation. Couplings between the front-side metal to the back-side metal also will not be negligible because of the thinned substrate (50 µm). As the frequencies of the paths that go through the TSVs increase, the inductive couplings and the skin effects are becoming more significant and should be taken into account.

A significant research effort has been made to respond to these upcoming challenges. The results were reported in the accurate modeling of the TSVs and modeling of their interactions [14] – [17]. The approaches taken are based either on accurate field-solver–based extraction of the TSVs and all their interactions or on developing the compact parametrized models that can then be used in extraction.

The model parameters include electrical characteristics of the all substrate layers as well as geometries of the TSVs and their neighborhood (TSV length, radius, oxide liner thickness, distance to other TSVs, etc.). An accurate description of the substrate layers and their doppant concentrations are needed from the foundries to be properly described for accurate modeling by the EDA tools.

The TSVs can exhibit some device-like properties; that is, TSV capacitance can be voltage-dependent, and several reports have provided the appropriate models [18]. There are different opinions on whether this will be important to model because this effect might be avoidable by appropriate process control that puts the TSV in a region of operation where capacitance is not voltage-dependant.

Die interface modeling has not been given much attention so far, but it has to be considered, especially in the case of direct face-to-face copper bonding but also when the dies are connected using the microbumps and copper pillars. The bump parasitic, bump interactions and their shielding effects are significant and should be taken into account. This would allow accurate net extraction and simulation across the stack.

One potentially very significant effect that is completely neglected is an inductive coupling between the stacked dies. The dies are closely vertically stacked and inductive interactions should be taken into account.

Also, very important and often neglected in the research community is that the generated solutions need to be integrated into the existing verification flows that are used for analog, digital and mixed signal designs verifications. Accuracy of the models, which is now the main focus of the

research is very important but is not of much use if it takes too much time to extract or cannot be simulated because of either large netlist size or incompatibilities of the formats.

Performance of the 3D-IC circuits can be significantly affected by uneven or excessive chip temperature [19], or because of stress related to the 3D stacking, as are die processing, the TSVs and the microbumps used to stack the chips [21]. More work and true cooperation between the design houses, EDA companies and the foundries is needed to properly address these issues and come up with the appropriate verifications flows.

VI. Conclusion

The existing methodology, the flows and the necessary tools to do accurate verification of TSV-based 3D-IC stacks of different configurations have been described here. An example was given to illustrate a true 3D-IC stack verification using a GDS based flow. The new challenges were presented and the development efforts and needs to respond to those challenges identified.

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