SILICON INTERPOSER FOR A 12X10 Gb/s ELECTRO-OPTICAL ENGINE

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ABSTRACT

The increasing transmission speeds in network switching, data storage, and super computing equipment makes it more and more difficult to use traditional electrical interconnects. Fiber optic links are a natural solution to this problem. Moving the optical fiber inside the box will demand smaller physical size modules that accommodate the increased density of high speed interconnects. This paper will present the design of small parallel optical transmitter and receiver assemblies that are surface mountable. They operate at 10 Gb/s today and are expected to migrate to 25 Gb/s in the near future.

The silicon interposer for this design provides top side electrical interconnects with flip chip mounting for a 1X12 Vertical Cavity Surface Emitting Laser (VCSEL) array die and a 1X12 VCSEL driver array die. A similar interposer is provisioned for a 1X12 photodetector array die and a 1X12 receiver array die. The solder pads on the VCSEL and photodetector arrays are precisely located relative to the optical apertures on each die. The silicon interposer has a matched set of solder pads that are precisely located relative to the end facets of the grooves that position the optical fibers in the final assembly.

When a wafer-scale solder reflow process is performed, surface tension of the molten solder pulls the corresponding pad arrays into precise alignment. The optical signals can be deflected 90 degrees into or out of the fibers by either cleaving the ends of the fibers at a 45 degree angle or by incorporating a 45 degree mirror at the end of the fiber grooves. This design eliminates the need for any additional optical coupling elements, and results in an arrangement, which has a very compact structure.

The input and output electrical traces for the ICs are routed on the top surface of the silicon interposer and are transferred to the back surface using through wafer vias. The populated interposer is diced from the wafer, and soldered to a printed circuit board or a high speed flex circuit.

Key words: FLIP-Chip Passive Alignment, Silicon Interposer, Wafer-Scale Processing, Vertical Cavity Surface Emitting Laser Array (VCSEL Array), VCSEL Driver Array IC, Interconnect Bandwidth Density, Laser Fiber Endface Cutting, Through Wafer Vias, Chip-to-World Interconnects

INTRODUCTION

Wafer-scale processing methods are used to produce a Silicon Interposer which forms the base for the assembly of an electro-optic (e-o) engine for Chip-to-World Interconnects. These e-o engines offer outstanding Interconnect Bandwidth Density. Silicon interposers are produced with photolithography techniques which offer extremely precise features (grooves for positioning optical fibers and solder pad arrays for flip-chip mounting and accurately positioning the electrical and optical chips).

The electro-optic array transducer chips include Vertical Cavity Surface Emitting Lasers Arrays (VCSEL Arrays) and optical photodetector arrays. These array e-o chips can be quickly flip-chip mounted onto the silicon interposer using standard pick-and-place machines. After flip-chip mounting the associated VCSEL Driver Array ICs and detector array ICs, all of the chips can be precisely aligned by a wafer-scale reflow of the gold-tin solder pads used for the flip chip mounting.

The electrical I/O interconnects for the laser and detector arrays and the ICs are provided by traces on the top surface of the silicon interposer. The electrical traces from the interposer top surface are transferred to the interposer back surface using Through Wafer Vias. After dicing the populated silicon interposer from the wafer, assembly to laser cut optical fiber waveguides is performed.

The result is a right angle optical coupling arrangement giving a very compact structure. The electrical connections on the back side of the silicon interposer can be bonded to an electrical flex circuit or a printed circuit board. The result is a chip-to-world interconnect that is small in size and low in cost while offering a high speed package with improved optical
coupling efficiency as shown in Fig. 1.

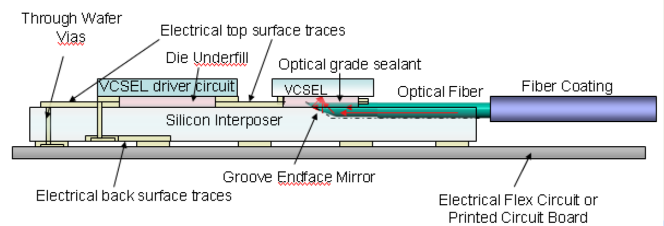

Figure 1. Silicon Interposer for VCSEL to Optical Fiber right angle coupling.

SILICON INTERPOSER PROCESSING

TE Connectivty, (formerly Tyco Electronics, a part of Tyco International) acquired AMP Inc. in Harrisburg, PA & Somerville, NJ and M/A-COM in Lowell & Burlington, MA) who developed a manufacturable process for mounting opto-electronic flip chip die onto silicon wafers. This work was presented at the Electronic Components and Technology Conference in 2001 [1]-[2]. US Patent 6,625,357 assigned to Tyco Electronics Corporation claims methods to fabricate devices having either mechanical seating or visually aligned fiducials. It also claimed the method of using matched solder metal pad arrays on the flip chip die and on the silicon interposer for passive solder reflow alignment [3]. This invention was extended to include additional methods as well as the product configurations that use matching solder metal pad arrays on the flip chips and the silicon wafer. US Patent 6,933,536 assigned to Tyco Electronics Corporation claims additional methods for passive solder reflow alignment using matched solder metal pad arrays in several product configurations. [4]

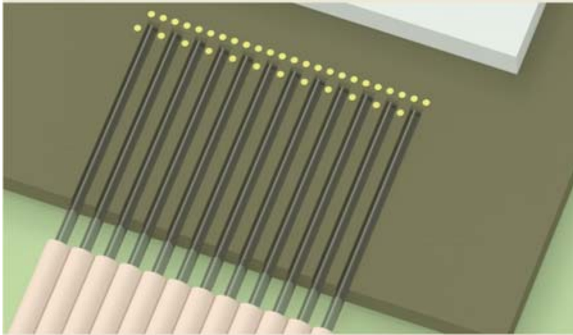

Figure 2. Silicon Interposer for VCSEL to Optical Fiber right angle coupling.

Passive die alignment by Gold / Tin solder reflow was presented at the 2003 M/A-COM Engineering Conference as an internal Tyco Electronics publication. [5] Figure 2 shows the metal pad array configuration for a VCSEL array die including the grooves for positioning laser cut optical fibers [6] under the VCSELs as shown in Figure 3 and Figure 4.

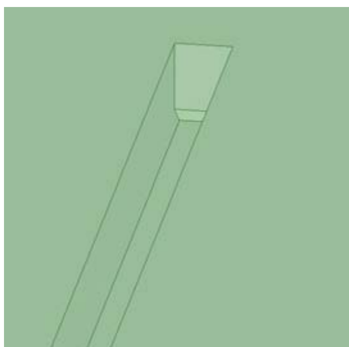

Figure 3. Silicon Interposer groove for optical fiber passive alignment.

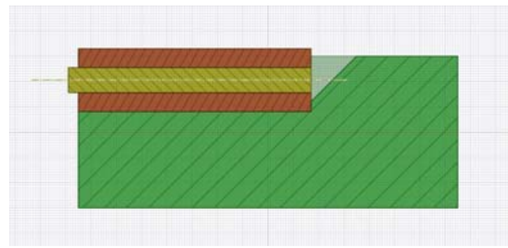

Figure 4. Optical fiber placed into groove

MIRROR COATING OF GROOVE END FACET

The groove end facet can be coated with a metal layer to form a right angle turning mirror as shown in Fig. 5 [9]. The optical coupling loss between the VCSEL and optical fiber is reduced and the optical return loss is improved when the airgap between the VCSEL or photodetector and the fiber is filled with an optical grade adhesive or sealant [7]-[8].

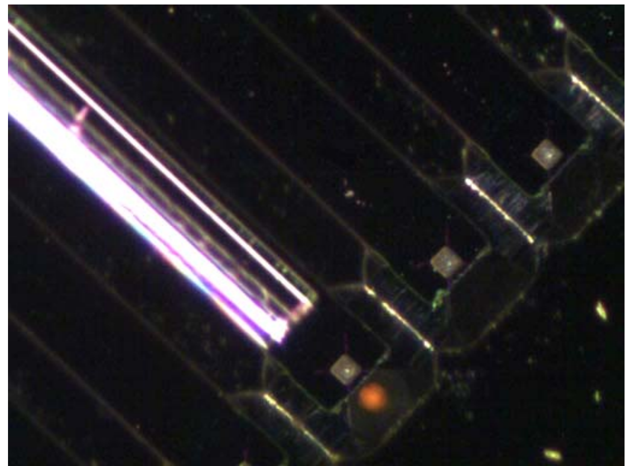

Figure 5. Groove End Facet Mirror with reflection of Optical Fiber Core

MIRROR REFLECTION COUPLING EFFICIENCY TESTING

In the real application it is not possible to directly measure the efficiency of the mirror because either the VCSEL or PIN diode is mounted over the mirror. To characterize the mirror a 50um fiber to fiber coupling measurement was done. The coupling results from this test will produce conservative values for the transmitter side because a typical VCSEL has an aperture of 8 to 10 um which is launched into a 50um fiber. At 10Gb/s the PIN diode will have an active area of 50 to 70um. The numerical aperture of a PIN is also much larger than the fiber so the measurement results will be slightly conservative for a receiver. A 1mW, 850nm laser was injected into a 50µm core multimode fiber. The opposite end of the fiber was inserted into a groove / trench on the interposer under test. A second 50µm core multimode fiber was held perpendicular to the groove over the mirror as shown in Fig. 6 below.

- The silicon substrate design incorporates a VCSEL that is flip chip mounted over the mirror. In this position it is not possible to measure the full VCSEL power to determine fiber coupling efficiency. To check performance of the mirror the VCSEL source was replaced by a 50um fiber.

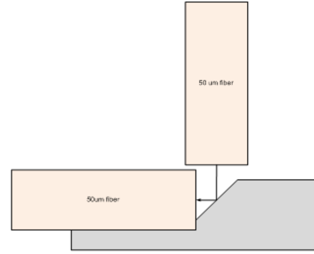

Figure 6. Fiber-to-Fiber Coupling Measurements

Laser light was coupled into the second fiber after being reflected off the aluminum coated, 45° degree facet in the groove / trench. The input and output powers were compared to establish the coupling efficiency/loss of the mirror system. Two groove / trench mirrors on each die were tested, and the results are shown in Table 1 below. Average coupling losses for trench 1 and trench 2 were 1.67 and 1.70dB respectively. Optical modeling of the VCSEL to fiber coupling showed that the actual expected coupling loss is 0.91dB. This assumes a worst case overfilled launch condition.

Input Power (mW) **0.960**

Sample	Description	Trench #1 (mW)	Trench #2 (mW)	dB #1	dB #2
1	S1,gap	0.700	0.683	1.372	1.479
2	S2,gap	0.674	0.665	1.536	1.594
3	S3,no gap	0.620	0.600	1.899	2.041
4	S3,gap	0.630	0.615	1.829	1.934
5	S3,no gap	0.609	0.622	1.977	1.885
6	S3,gap	0.648	0.612	1.707	1.955
7	S2,no gap	0.628	0.626	1.843	1.857
8	S1,no gap	0.660	0.670	1.627	1.562
9	S2,gap	0.711	0.712	1.304	1.298
10	S1,gap	0.680	0.695	1.498	1.403
11	S2,no gap	0.644	0.640	1.734	1.761
			Average Loss (dB)	1.666	1.706

Table 1. Mirror reflection coupling efficiency

INDEX MATCHING POLYMER ADHESIVE (IPA) TEST

In order to improve coupling efficiency, the mirror pit will be filled with an index matching polymer. To simulate this effect, two fibers were positioned as described above (i.e. one in the groove, and one above the mirror), and coupling was optimized. The pit was filled with IPA, and the output power measurements were compared. The results are shown in Table 2.

w/o IPA	w/ IPA	% increase
0.678	0.714	5.310
0.648	0.670	3.395

Table 2. Mirror reflection coupling efficiency improvement with the addition of IPA

ATTENUATION VERSUS DISTANCE

To check the sensitivity of fiber insertion depth to coupled power the same two fiber setup was used. The position of the vertical fiber was optimized for coupled power and the light emitting fiber was stepped away from the mirror in 20 µm increments. The output power was measured at each discrete step, and the results are shown in the Figure 7 plot below. The fiber can be moved away a distance of 250um before the coupling drops by 3dB.

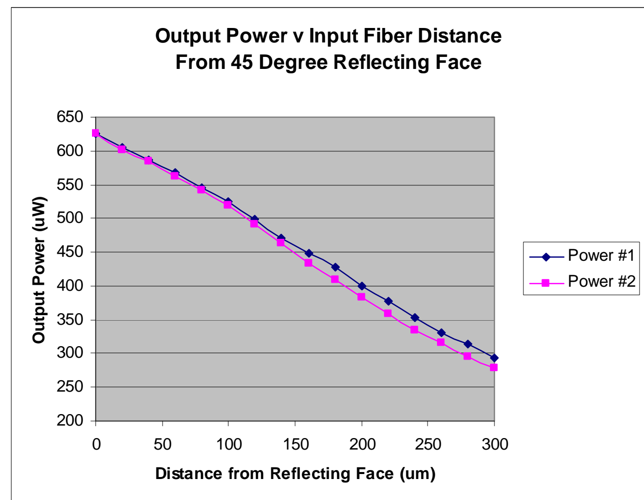

Figure 7. Fiber-Mirror-Fiber Coupling Measurements

The sensitivity to fiber insertion depth in a prior design that utilized a 45 degree angle cleaved on the ends of the fibers made it difficult to achieve uniform coupling with fiber arrays as shown in figure 8.

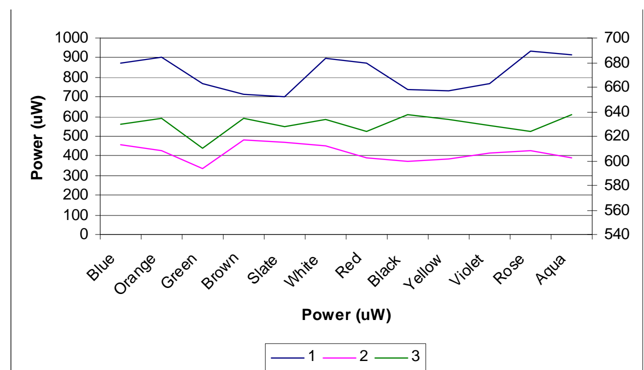

Figure 8. Power measurements using 3 different unplated 45 degree angle cleaved fibers.

In addition the 45 degree cleaved fibers required a reflective coating on the ends so that an underfill material could be used between the active optical devices and the fibers.

Fibers with laser cut ends and reflective coationg are shown below in Figure 9.

Figure 9. Left is close up of fiber end showing emitted light. Top is underside of fiber with reflective coating. Bottom is top of angle cleaved fibers.

Optical simulations for this arrangement can be seen in figure 10. Lateral tolerance for this arrangement is an order of magnitude greater than the mirrored trench.

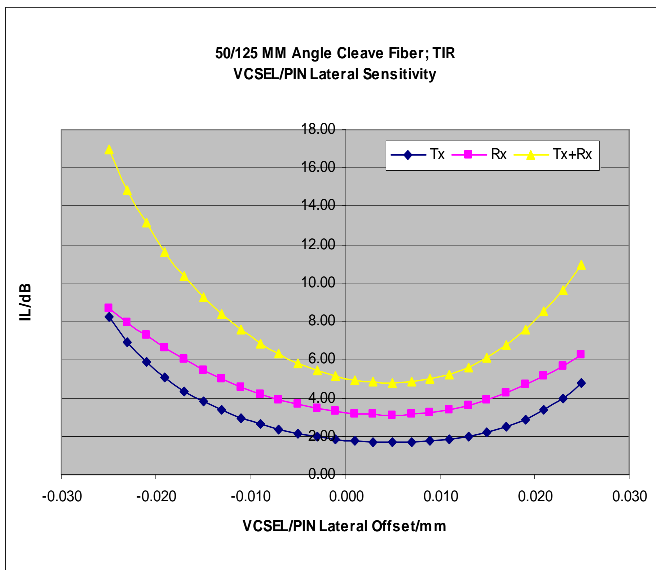

Figure 10. Lateral positional loss of angled cleave fiber.

ELECTRICAL PERFORMANCE

At data rates of 10 and 25 Gb/s it is critical that the electrical layout of the silicon substrate has controlled impedance traces and low crosstalk between the traces. Proper impedance control must also be maintained for the signal going through the silicon substrate (TSV) to the bottom contacts. The target impedance is 90 ohms. Figure 11 shows TDR simulation results where an impedance of better than 90 ohms +/- 10% was achieved for the connection between the top of the silicon substrate and the Printed Circuit Board (PCB) that the interposer is mounted on.

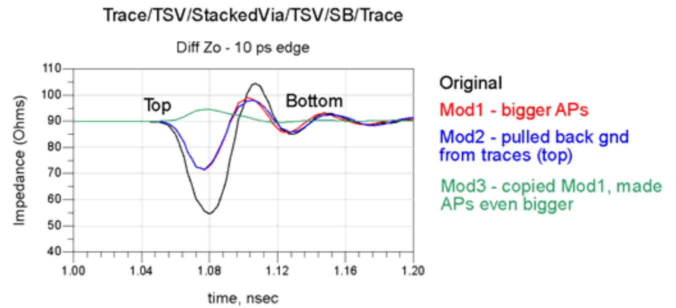

Figure 11. TDR plot of TSV and PCB interconnect.

A test vehicle consisting of two silicon interposers, one 12 lane transmitter and one 12 lane receiver, was formed by mounting the interposers to a small PCB that mates to an edge card connector as shown in Figure 12. Figure 13 is a top view of one of the two interposers that were mounted on opposite sides of the printed circuit board. Ribbon fibers were attached to the trenches in the silicon substrate. The size of the PCB is 14.7 x 30 mm. Only 8 of the 12 transmitter and receiver lanes were routed to be compatible with the electrical connector.

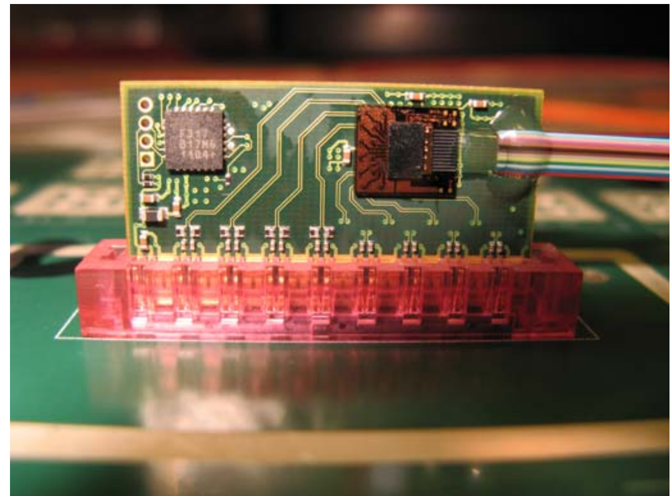

Figure 12. Silicon interposers mounted to test PCB.

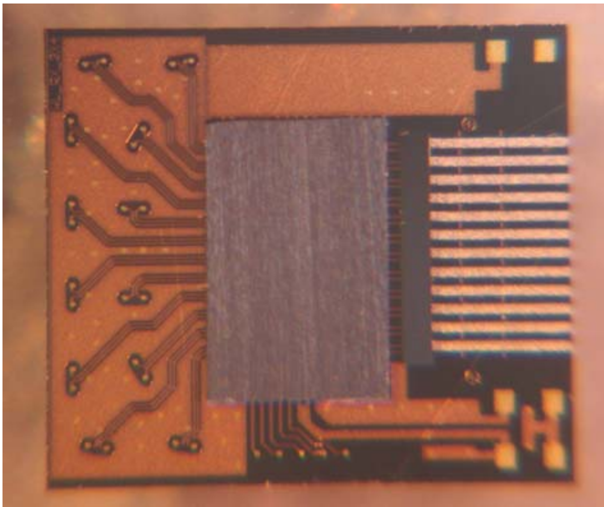

Figure 13. Top side of silicon interposer with flip mounted components.

CONCLUSION

Electrical eye pattern measurements were made at the output of the optical receiver by looping back the optical transmitter output channels to the receiver input channels on the test PCB. The components selected were designed for 10Gb/s operation. Eye patterns were also taken at 12.5 and 14Gb/s to see the rate at which the eye opening degrades. An open eye was still achievable at 14Gb/s as seen in Figures 14 to 17. The silicon interposer for this design performed well in the testing and should provide a solid platform for next generation higher speed devices.

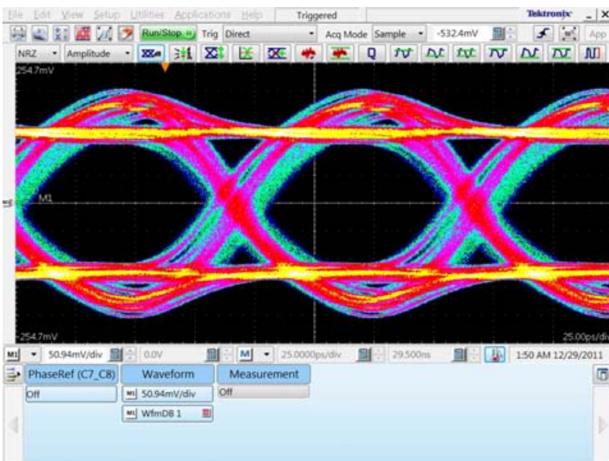

Figure 14. 10Gb/s 2^7-1 PRBS

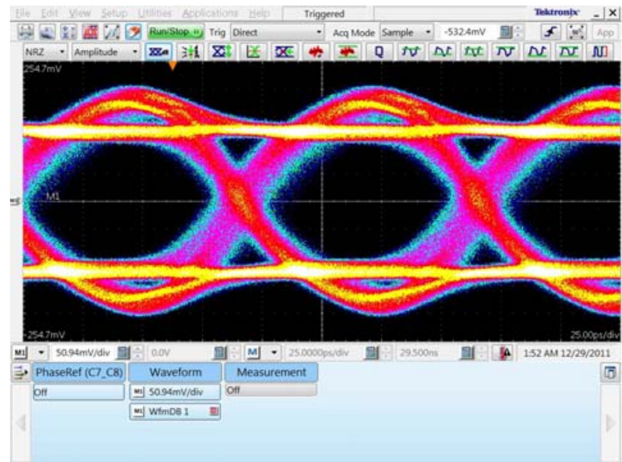

Figure 15. 10Gb/s 2^31-1 PRBS

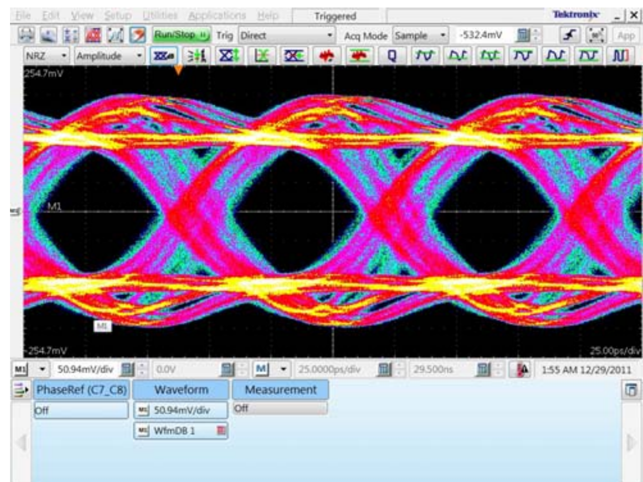

Figure 16. 12.5Gb/s 2^7-1 PRBS

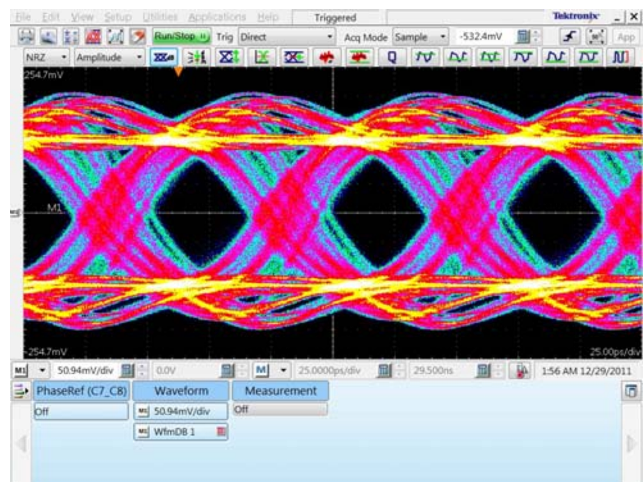

Figure 17. 14Gb/s 2^7-1 PRBS

ACKNOWLEDGEMENTS

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Sample preparation and testing was performed by Bob Fair of TE Connectivity.

AMP, M/A-COM, Tyco Electronics, and TE Connectivity are trademarks of Tyco Electronics Corporation.

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